Negative output 200mA LDO
Monolithic IC MM1898 Series

Outline

This IC is a low noise negative output 200mA LDO by bipolar process. The target applications by noise reduction pin are for a power supply of highly sensitive image sensor. The output range is from −0.9V to −5.0V (0.1V steps), it can use to the negative power supply of CMOS image sensor.

Features

1.	Input voltage range	−2V to −10V
2.	Output voltage range	−0.9V to −5.0V
3.	Output voltage accuracy	V_{OUT}±1% (V_O<−1.5V)
		V_{OUT}±15mV (−1.5V≦V_O≦−0.9V)
4.	Maximum output current	200mA
5.	Current consumption	3μA typ. (OFF)
		160μA typ. (No-Load)
6.	Dropout voltage	0.5V typ. / 0.8V max. (I_O=200mA)
7.	Line regulation	0.01%/V typ.
		0.10%/V max.
8.	Load regulation	15mV typ. / 100mV max. (I_O=1mA to 200mA)
9.	Ripple rejection	70dB typ. (f=1kHz)
10.	Output noise voltage	30μVrms typ. (V_O=−1.4V, Cn=0.01μF)
11.	Output rise time	5ms typ. (Cn=0.01μF, I_{OUT}=0mA)

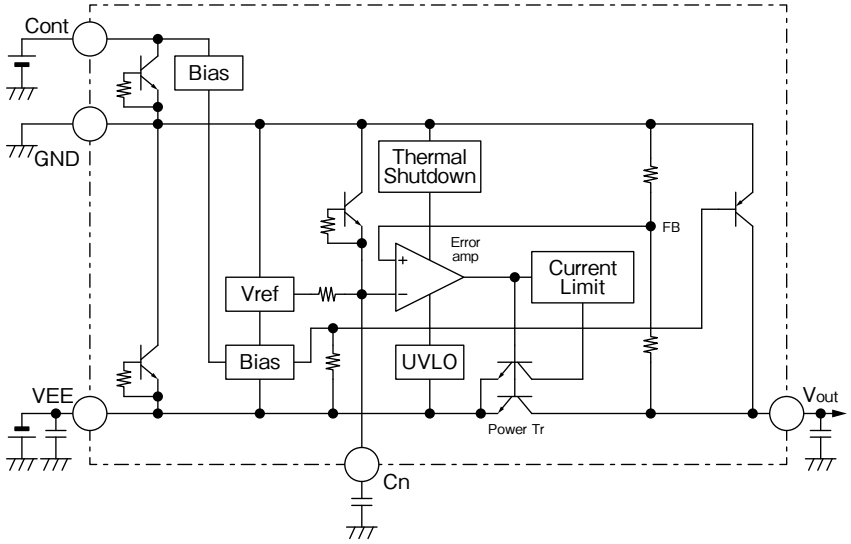
Package

SOT-25A
SSON-6A

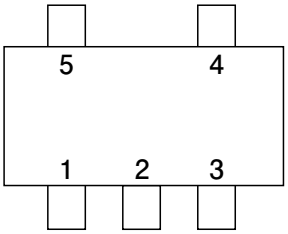
Applications

1. Image sensor
2. LCD

Block Diagram

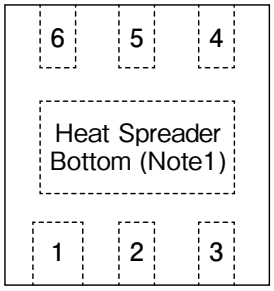


Pin Assignment



SOT-25A
(TOP VIEW)

1	GND
2	VEE
3	Cont
4	Cn
5	VOUT



SSON-6A
(TOP VIEW)

1	Cont
2	GND
3	VEE
4	VOUT
5	NC
6	Cn

Note1 : Heat Spreader Bottom with VEE.
Don't connect with GND.

Pin Description

SOT-25A

Pin No.	Pin name	Functions
1	GND	Ground pin
2	VEE	Negative voltage input pin
3	Cont	Control pin Vcont=H : Output ON Vcont=L : Output OFF
4	Cn	Reducing noise pin with capacitor pin
5	VOUT	Negative voltage output pin

SSON-6A

Pin No.	Pin name	Functions
1	Cont	Control pin Vcont=H : Output ON Vcont=L : Output OFF
2	GND	Ground pin
3	VEE	Negative voltage input pin
4	VOUT	Negative voltage output pin
5	NC	No connection
6	Cn	Reducing noise pin with capacitor pin

Absolute Maximum Ratings (Except where noted otherwise Ta=25℃)

Item	Symbol	Ratings		Units
Supply voltage	VEE	−12 to +0.3		V
Control voltage	Vcont	−0.3 to +5.0		
Output current	Iout	0 to 400		mA
Junction Temperature	TjMAX	125		℃
Storage Temperature	Tstg	−55 to +125		
Power Dissipation	Pd	SOT-25A	560(Note2)	mW
		SSON-6A	1000(Note2)	

Note2 : JEDEC51-7 Standard 114.3mm×76.2mm, t=1.6mm

Recommended Operating Conditions (Except where noted otherwise Ta=25℃)

Item	Symbol	Ratings	Units
Operating Ambient temperature	Topr	−40 to +85	℃
Operating Voltage	Vop	−10 to −2	V
Output Current	Iop	0 to 200	mA

Electrical Characteristics 1 (Except where noted otherwise VEE=VOUT(typ.)-1V, Iout=1mA, Vcont=1.6V, Ta=25℃)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Input current consumption (OFF)	IEEOFF	VEE=-5V, Vcont=0V		3	8	μA
No-Load input current consumption	IEE	Iout=0mA		160	240	
Output voltage (Note3)	VOUT	VOUT≦-1.5V	×1.01		×0.99	V
		VOUT>-1.5V	-0.015		+0.015	
Dropout voltage	Vio	VEE=Vo+0.2V, Iout=200mA		0.5	0.8	
Line regulation	Vline	VOUT≦-1.0V, VEE=VOUT-1 to -10V		0.01	0.10	%/V
		VOUT=-0.9V, VEE=-2 to -10V				
Load regulation	Vload	Iout=1m to 200mA		15	100	mV
Vout temperature coefficient (Note4)	⊿VOUT/⊿T	Ta=-40 to +85℃		±100		ppm/℃
Ripple rejection (Note4)	RR	f=1kHz, Vripple=0.5A, Iout=10mA, Cn=0.01μA		70		dB
Output noise voltage (Note4)	Vn	VOUT=-1.4V, fBW=10k to 100kHz, Iout=10mA, Cn=0.01μA		30		μVrms
Cont pin input current	Icont	Vcont=1.6V		4	12	μA
Cont pin High Threshold level	VcontH	VOUT : ON	1.2			V
Cont pin Low Threshold level	VcontL	VOUT : OFF			0.3	
Output rise time	Tr	Cn=0.01μF, Iout=0mA (Note5)		5		ms
UVLO detective voltage	VUVLO		-1.85	-1.75	-1.65	V
UVLO hysteresis voltage	⊿VUVLO			0.15		
Discharge current	Idis	VEE=-5V, Vcont=0V		4		mA

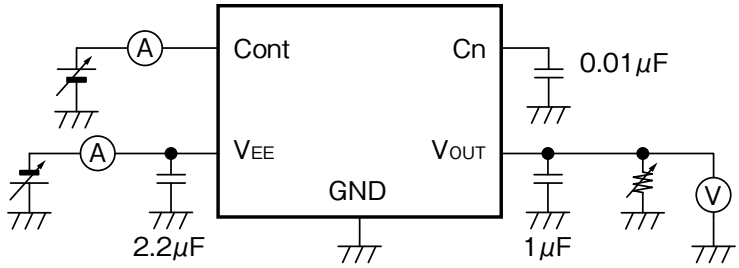
Note3 : Please refer to another page.
Note4 : The parameter is guaranteed by design.
Note5 : Vcont=H to 90% of Vout (Typ.)

Electrical Characteristics 2

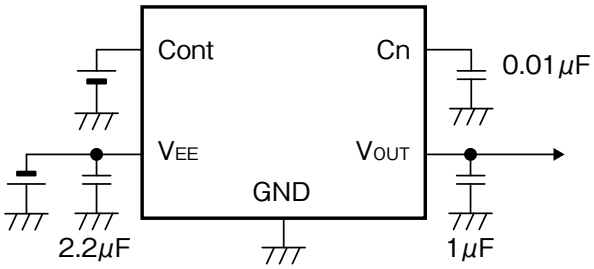
(Except where noted otherwise VEE=VOUT(typ.)−1V, Iout=1mA, Vcont=1.6V, Ta=25℃)

Output voltage	Measurement Conditions	Output Voltage (V)		
		Min.	Typ.	Max.
−0.9	Iout=1mA	−0.915	−0.900	−0.885
−1.0		−1.015	−1.000	−0.985
−1.1		−1.115	−1.100	−1.085
−1.2		−1.215	−1.200	−1.185
−1.3		−1.315	−1.300	−1.285
−1.4		−1.415	−1.400	−1.385
−1.5		−1.515	−1.500	−1.485
−1.6		−1.616	−1.600	−1.584
−1.7		−1.717	−1.700	−1.683
−1.8		−1.818	−1.800	−1.782
−1.9		−1.919	−1.900	−1.881
−2.0		−2.020	−2.000	−1.980
−2.1		−2.121	−2.100	−2.079
−2.2		−2.222	−2.200	−2.178
−2.3		−2.323	−2.300	−2.277
−2.4		−2.424	−2.400	−2.376
−2.5		−2.525	−2.500	−2.475
−2.6		−2.626	−2.600	−2.574
−2.7		−2.727	−2.700	−2.673
−2.8		−2.828	−2.800	−2.772
−2.9		−2.929	−2.900	−2.871
−3.0		−3.030	−3.000	−2.970
−3.1		−3.131	−3.100	−3.069
−3.2		−3.232	−3.200	−3.168
−3.3		−3.333	−3.300	−3.267
−3.4		−3.434	−3.400	−3.366
−3.5		−3.535	−3.500	−3.465
−3.6		−3.636	−3.600	−3.564
−3.7		−3.737	−3.700	−3.663
−3.8		−3.838	−3.800	−3.762
−3.9		−3.939	−3.900	−3.861
−4.0		−4.040	−4.000	−3.960
−4.1		−4.141	−4.100	−4.059
−4.2		−4.242	−4.200	−4.158
−4.3		−4.343	−4.300	−4.257
−4.4		−4.444	−4.400	−4.356
−4.5		−4.545	−4.500	−4.455
−4.6		−4.646	−4.600	−4.554
−4.7		−4.747	−4.700	−4.653
−4.8		−4.848	−4.800	−4.752
−4.9		−4.949	−4.900	−4.851
−5.0		−5.050	−5.000	−4.950

Measuring Circuit



Application Circuit



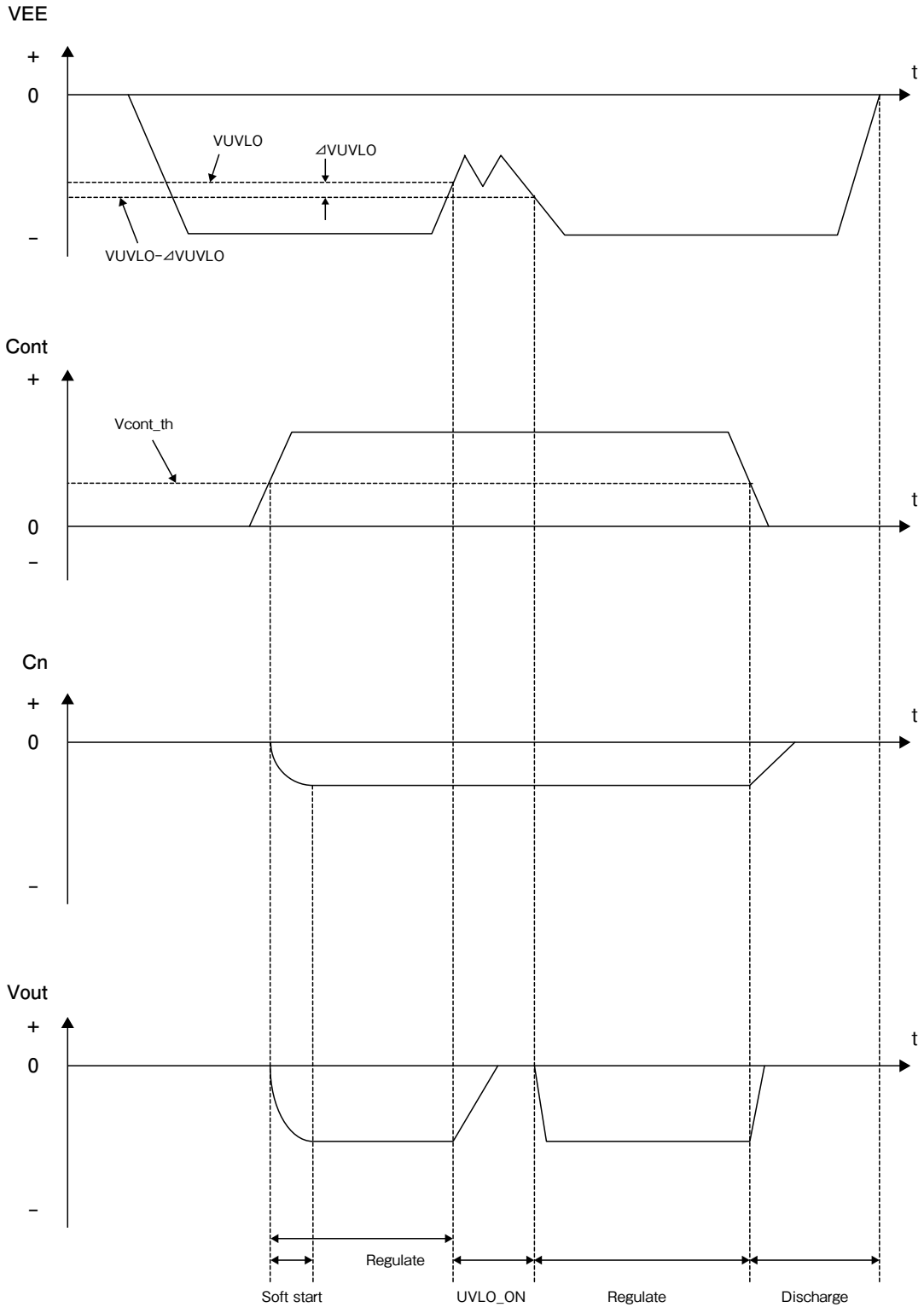
(Reference example of external parts)

· Output capacitor Ceramic capacitor 1.0μF (2.2μF for Vo≧-1.1V) *Temperature Characteristics : B

· Input capacitor Ceramic capacitor 2.2μF *Temperature Characteristics : B

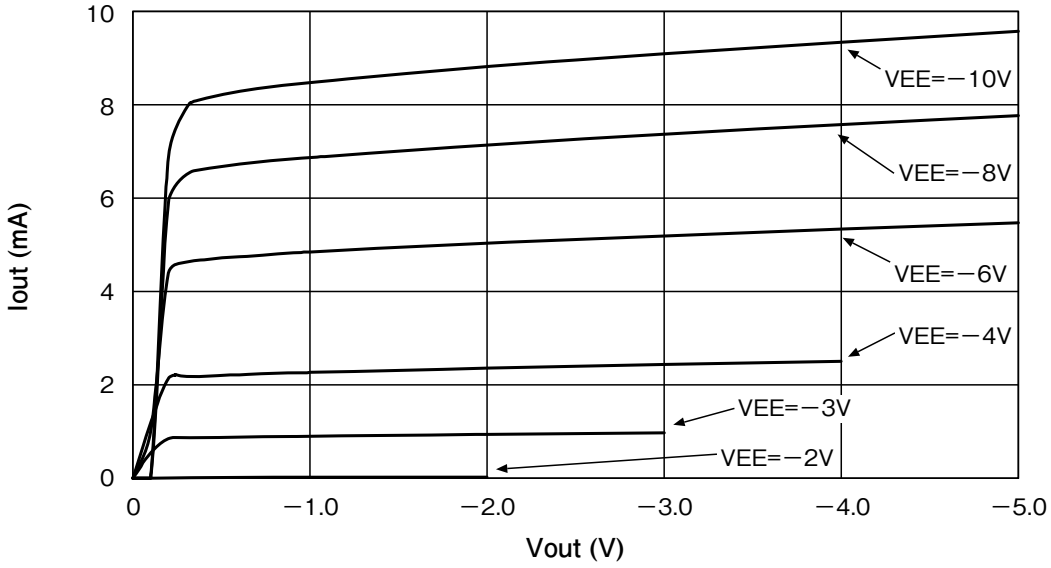
· In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, we shall not be liable for any such problem, nor grant a license therefore.

Timing Chart



Discharge Current Depending on Power Supply

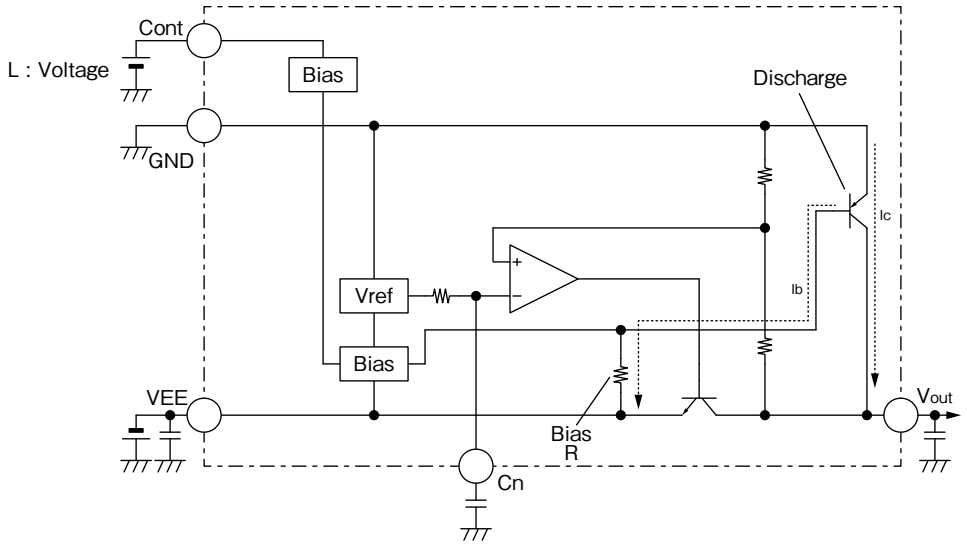
Discharge current depend on power supply VEE.
Reference to Below current characteristics.
In case of discharge current being low, contact us.



Discharge Circuit Current

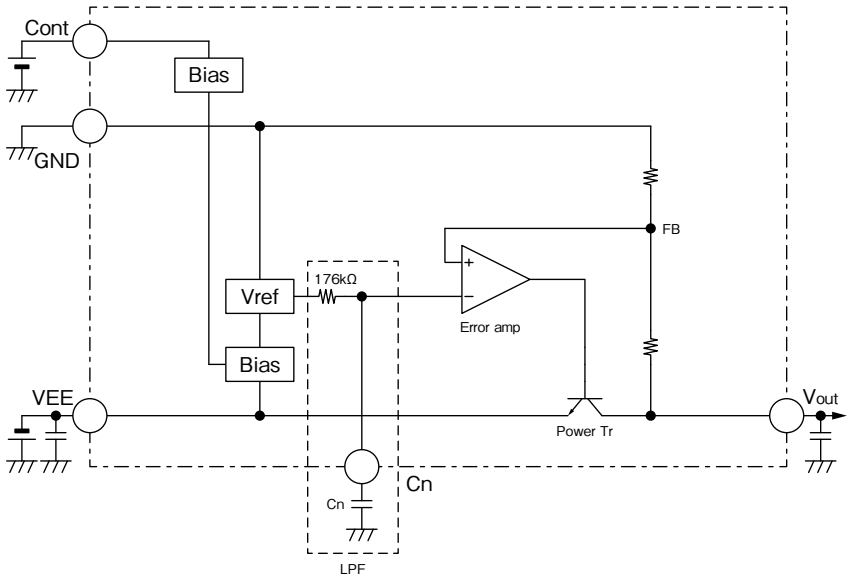
Discharge current is collector current of discharge element in IC.
Collector current Ic is hfe times as many as base current Ib, equation (1).
Base current Ib depend on bias resistance R, equation (2).
Collector current express equation (3).
Discharge current (collector current) depend on VEE voltage.
And base current is input current (OFF).

Ic=hfe×Ib ・・・(1)
Ib=(VEE−0.7)÷R ・・・(2)
Ic=hfe×(VEE−0.7)÷R ・・・(3)



Cn Pin

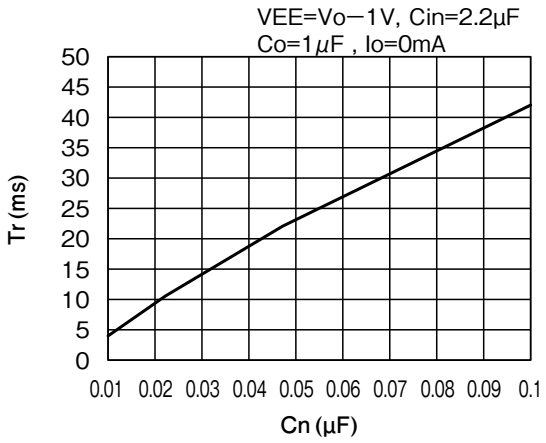
Cn pin is connected with resistance 176kΩ in IC.
LPF is composed of capacitor, Cn noise is reduced and VOUT noise is reduced too.
This IC feedback FB that is divided from VOUT by resistance equal with Cn voltage.
Noise of FB is feedbacked equal with noise of Cn too.
So noise of VOUT depend on noise of Cn. The capacitor of Cn pin more than 0.01μF is recommended.
If Cn pin influence by noise for outside, noise of VOUT pin is bad characteristics.



Output rise time

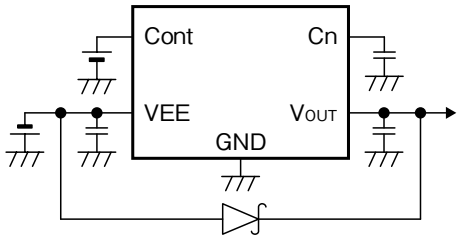
MM1898 starting soft start in cause of outside capacitor connected with Cn pin.
Cn voltage start slowly in course of LPF.
FB voltage is feedback equal to Cn voltage, therefore FB and Vout voltage start slowly.
Output rise time Tr depend on capacitor Cn that is connected with Cn pin.
About output rise time, refer to below equation and characteristics.

$$Tr\ [ms] \fallingdotseq 405 \times Cn\ [\mu F]$$



NOTE

1. There is a possibility with deterioration and destruction of IC when using it exceeding the absolute maximum rating. The absolute maximum rating, Never exceed it.
   The functional operation is not assured.
2. There is a possibility that it becomes impossible to maintain this performance and reliability IC original when using it exceeding recommended operation voltage.
   Please use it in recommended operation voltage.
3. Due to restrictions on the package power dissipation, the output current value may not be satisfied. Attention should be paid to the power dissipation of the package when the output current is large or the voltage between Input and Output is high.
4. The output capacitor is required between output and GND to prevent oscillation.
5. The ESR of capacitor must be defined in ESR stability area.
   It is possible to use a ceramic capacitor without ESR resistance for output.
   The ceramic capacitor must be used more than 1.0μF and B temperature characteristics.
   The ceramic capacitor must be used more than 2.2μF and B temperature characteristics for Vo≧1.1V.
6. The wire of VEE and GND is required to print full ground plane for noise and stability.
7. The input capacitor must be connected a distance of less than 1cm from input pin.
8. In case the output voltage is above the input voltage, the overcurrent flow by internal parasitic diode from output to input.
   In such application, the external bypass diode must be connected between output and input pin.

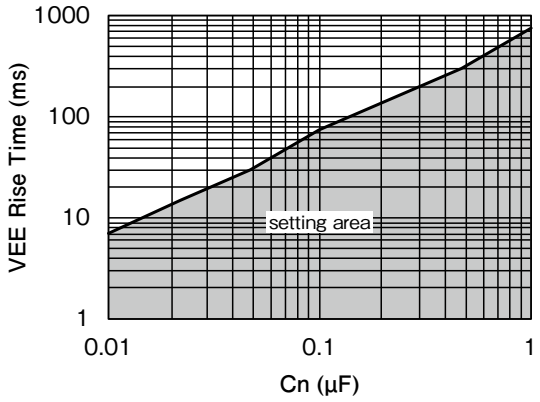


9. It is able to an unstable operation when you use the capacitor with intense capacitance change.
   The capacitor has the dependency at the power-supply voltage and the temperature.
   The capacity value changes by the environment used. Please evaluate IC in the set.
10. The IC has the thermal shutdown protection.
11. This IC will limit the output current with the overcurrent protection circuit when the overcurrent and the output do short-circuit. However, IC generates heat because of the substrate and use conditions and there is a possibility of destroying it exceeding a permissible loss.
    The characteristic changes depending on the substrate condition.
    Please evaluate IC in the set.
12. Cont pin control ON/OFF of this IC. Cont pin is used to input plus voltage.
    If this pin is open, this IC is OFF.

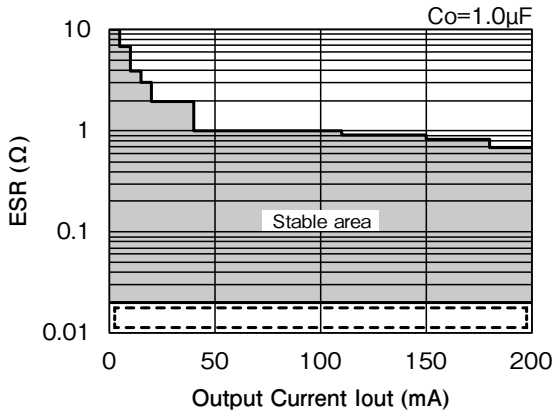
    ON : 1.2V≦Vcont≦5.0V
    OFF : 0V≦Vcont≦+0.3V

13. The overshoot might be generated in UVLO releasing for low output voltage rank.
It is above fanction When VEE rise time is late and strating by not Cont but VEE So set the setting area in below graf.

Condition : VEE=0→-2V, Vcont=1.6V, Ta=-40℃ to +85℃



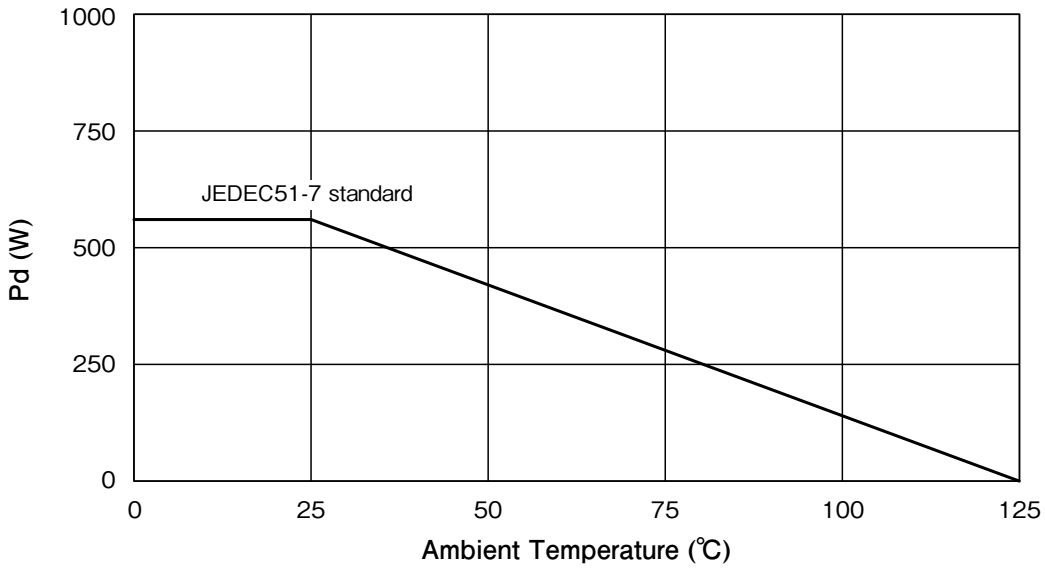
14. It is no data in under 0.02Ω of ESR characteristics. (dotted line area)
Don't be measured in this area because ceramic capacitor contain 0.02Ω in parts self.
Ceramic capacitor only can be used without ESR resistance parts.
Please evaluate IC in the set if the capacitor that is low resistance used.



About Power Dissipation

The Power dissipation change if board to mount IC change because radiative heat fix at board.It is reference data below, Evaluate IC in the set.

1. JEDEC51-7 standard
   Board size 114.3mm×76.2mm t=1.6mm Copper foil area 80%
   Power dissipation 560mW Ta=25°C (It is reference value measured by JEDEC51-7 standard.)

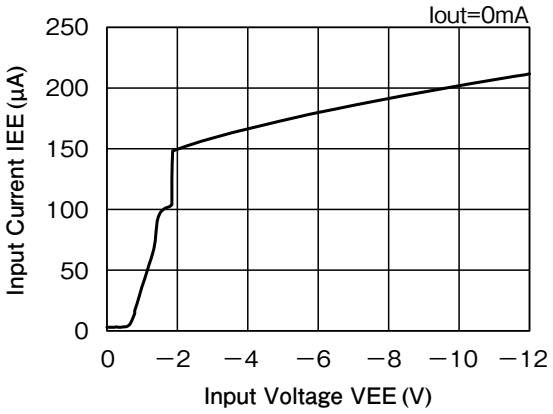


It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate).
By increasing these copper foil pattern area of PCB, Power dissipation improves.

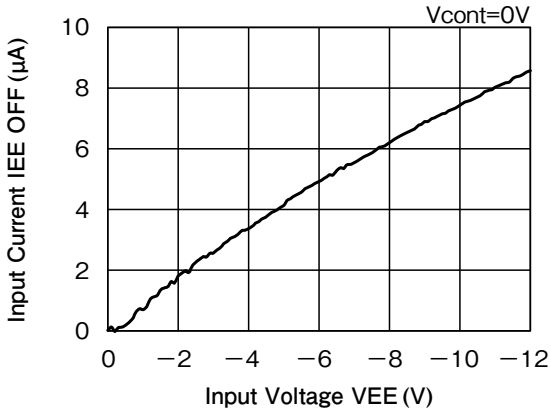
Characteristics (−0.9V)

(Except where noted otherwise VEE=VOUT(Typ.)−1V, Iout=1mA, Vcont=1.6V, Ta=25℃, VEE=−2V at VOUT=−0.9V)

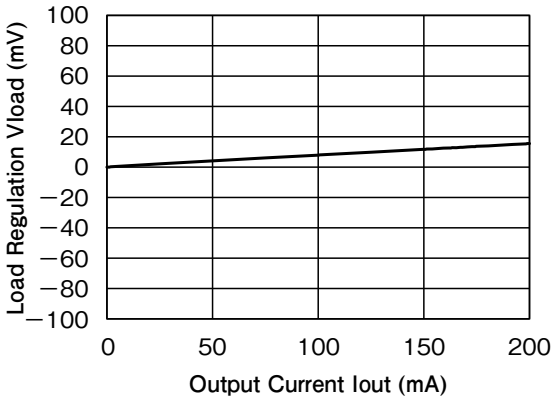
Input voltage − Input current



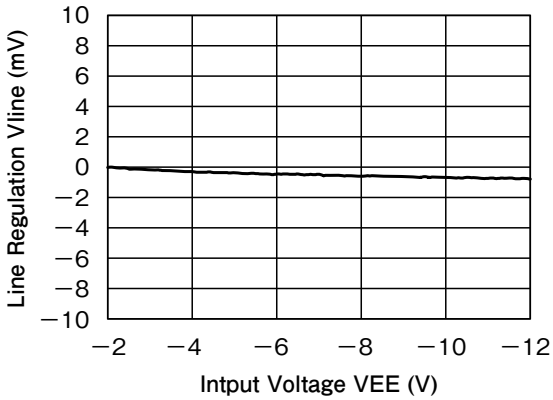
Input voltage − Input current



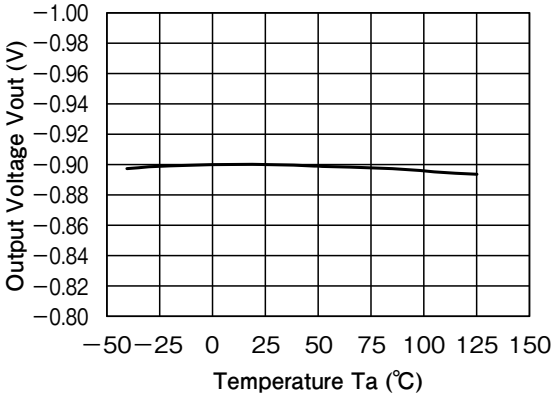
Load regulation



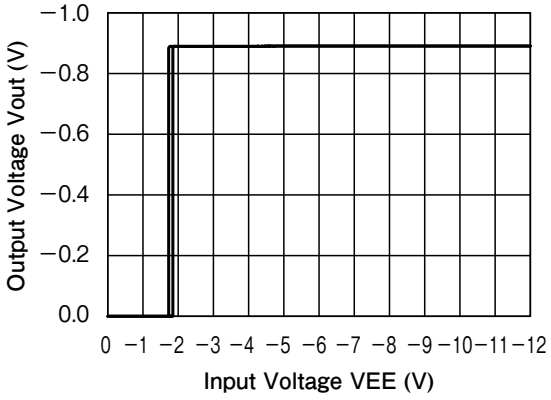
Line regulation



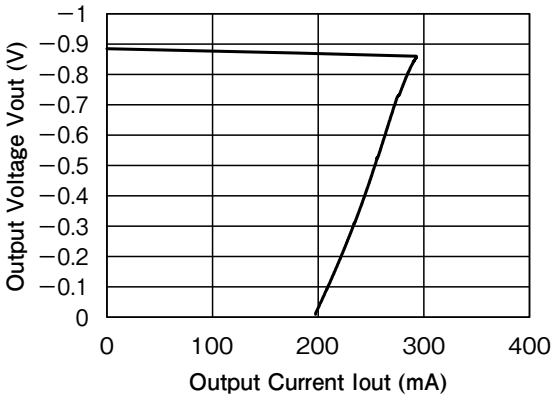
Output Voltage Temperature Coefficient



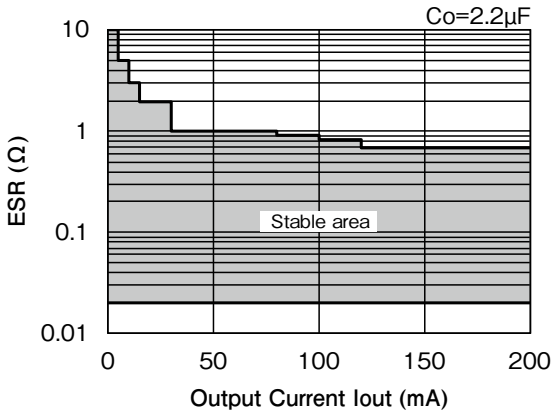
Input voltage − Output voltage



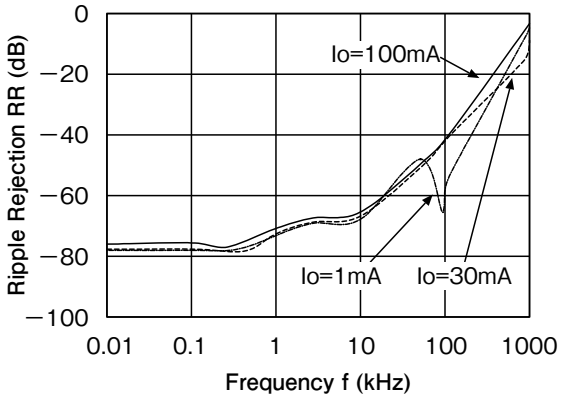
Output current – Output voltage



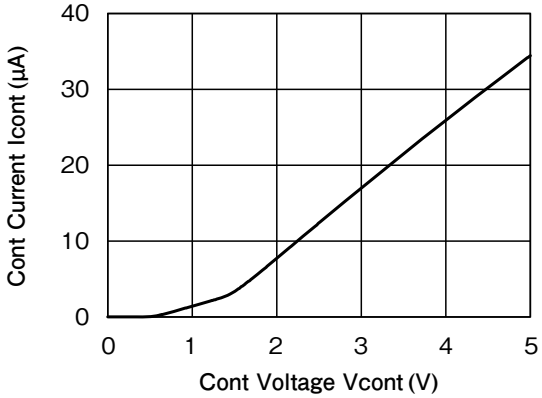
ESR stable area



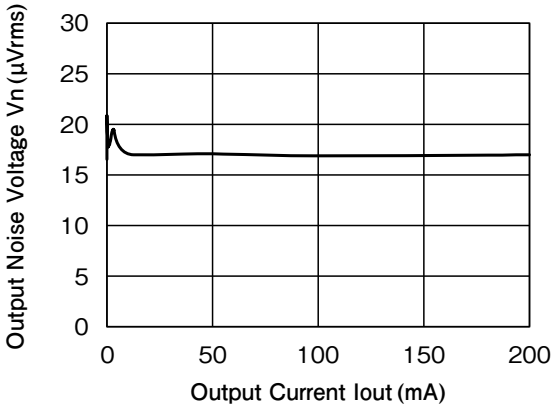
Ripple Rejection



Cont voltage – Cont current

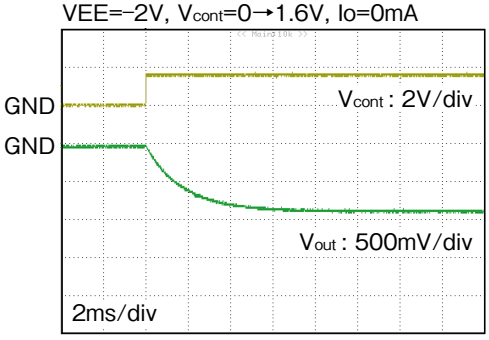


Cont voltage – Cont current

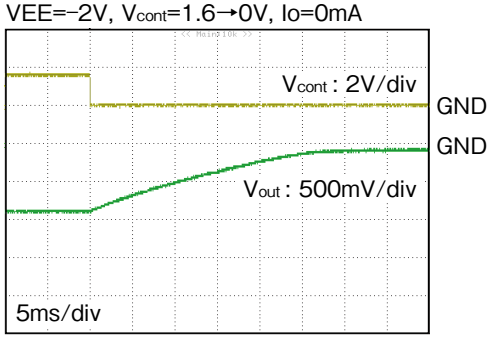


Cont rise characteristics

VEE=−2V, V_{cont}=0→1.6V, Io=0mA

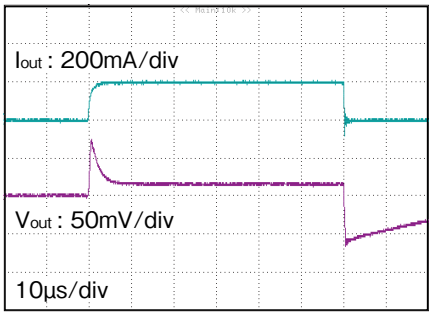


VEE=−2V, V_{cont}=1.6→0V, Io=0mA

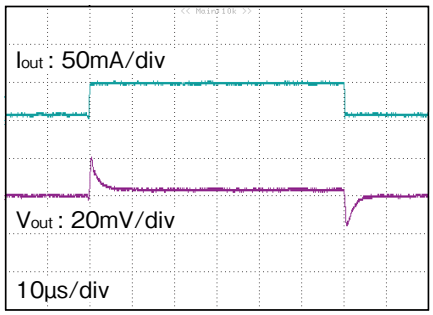


Load transient characteristics

I_{out}=0.1mA⇔200mA



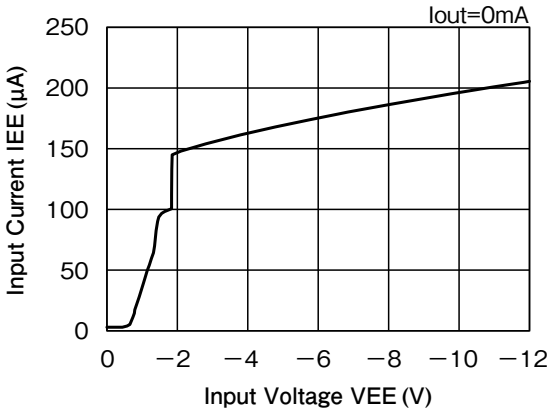
I_{out}=10mA⇔50mA



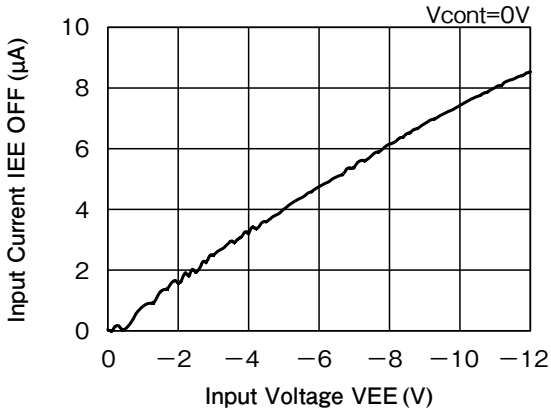
Characteristics (−1.4V)

(Except where noted otherwise VEE=VOUT(Typ.)−1V, Iout=1mA, Vcont=1.6V, Ta=25℃, VEE=−2V at VOUT=−0.9V)

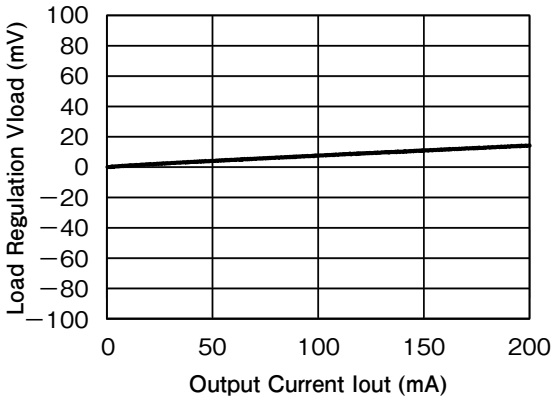
Input voltage − Input current



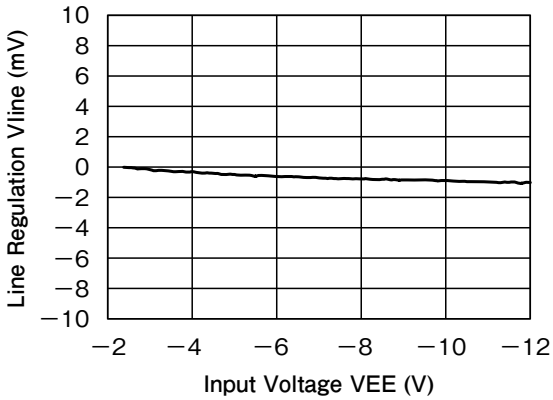
Input voltage − Input current



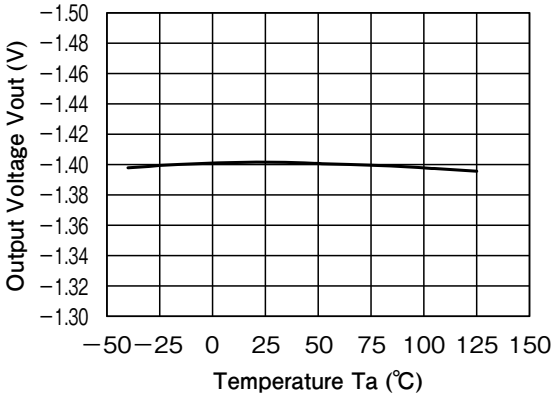
Load regulation



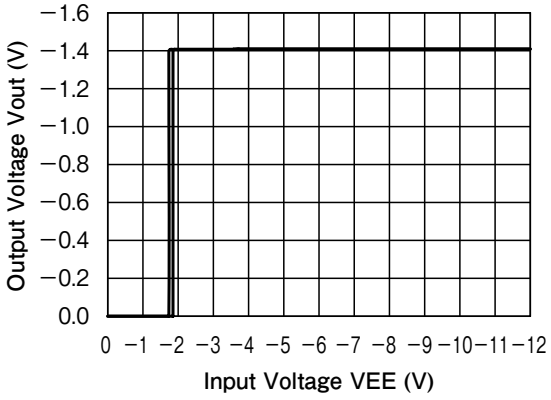
Line regulation



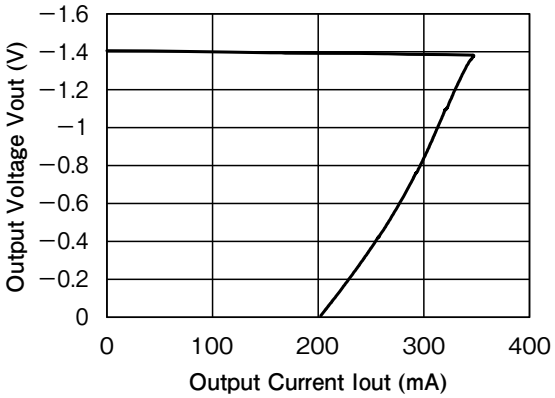
Output Voltage Temperature Coefficient



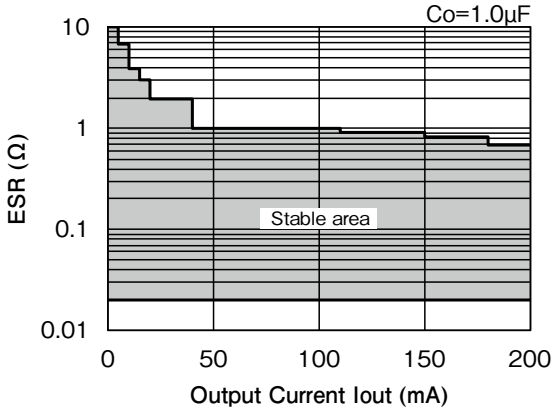
Input voltage − Output voltage



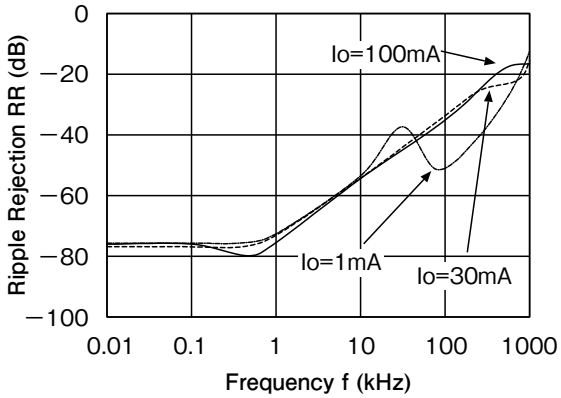
Output current – Output voltage



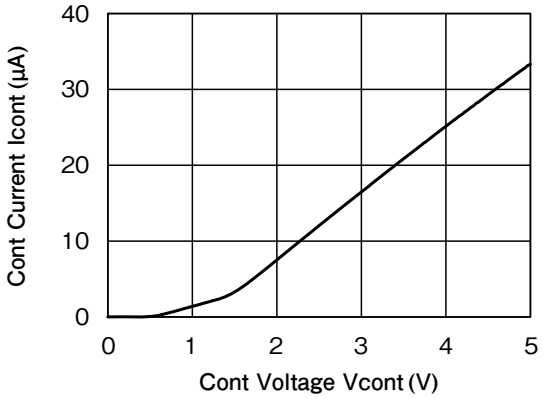
ESR stable area



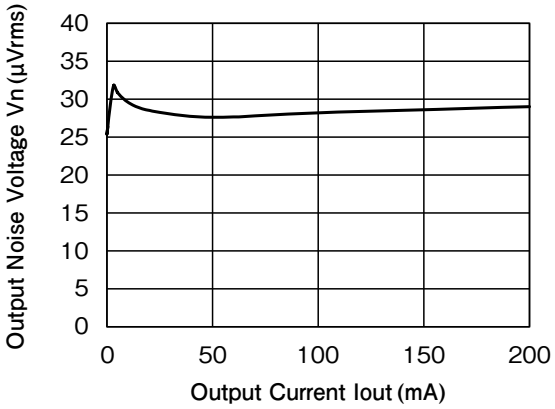
Ripple Rejection



Cont voltage – Cont current

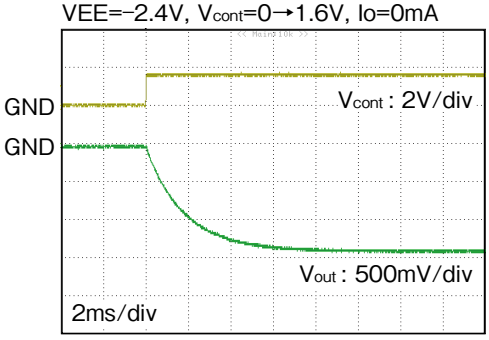


Cont voltage – Cont current

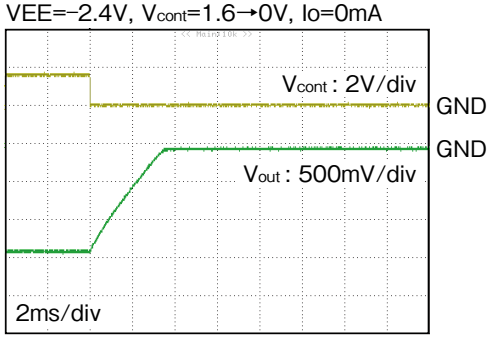


Cont rise characteristics

VEE=−2.4V, V_{cont}=0→1.6V, Io=0mA

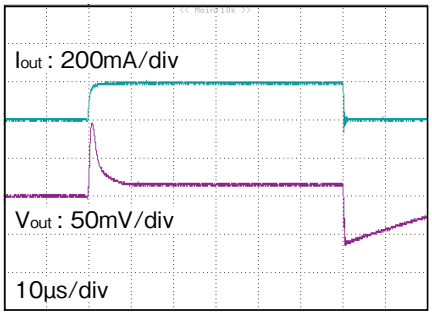


VEE=−2.4V, V_{cont}=1.6→0V, Io=0mA

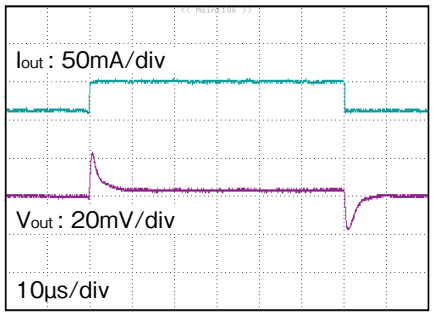


Load transient characteristics

I_{out}=0.1mA⇔200mA



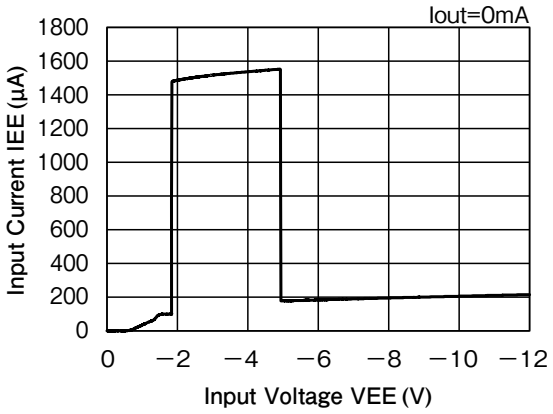
I_{out}=10mA⇔50mA



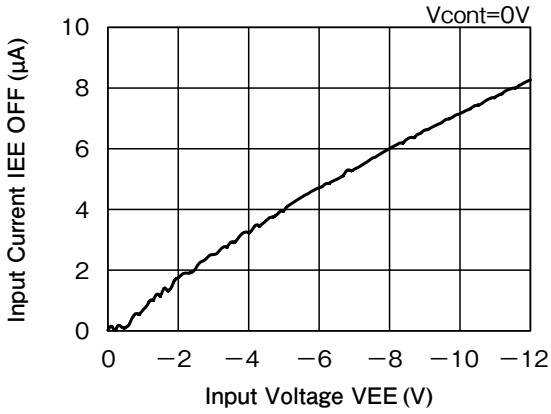
Characteristics (−5.0V)

(Except where noted otherwise VEE=VOUT(Typ.)−1V, Iout=1mA, Vcont=1.6V, Ta=25℃, VEE=−2V at VOUT=−0.9V)

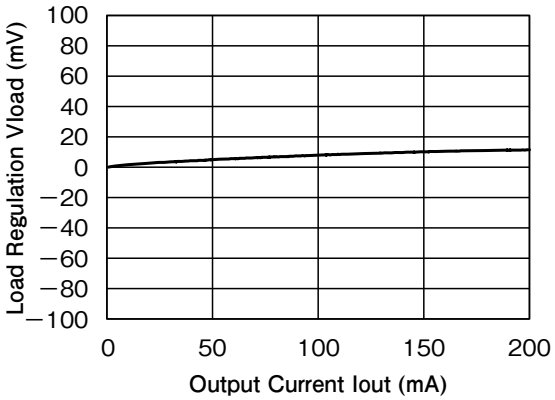
Input voltage − Input current



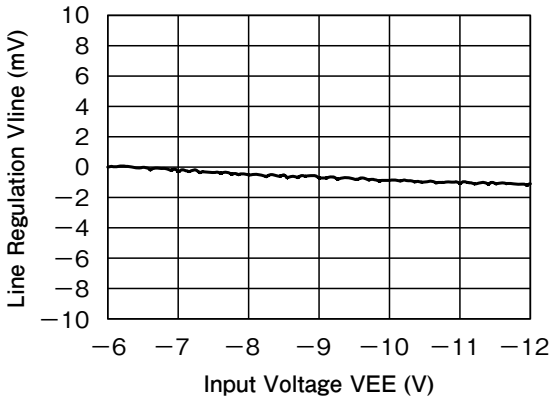
Input voltage − Input current



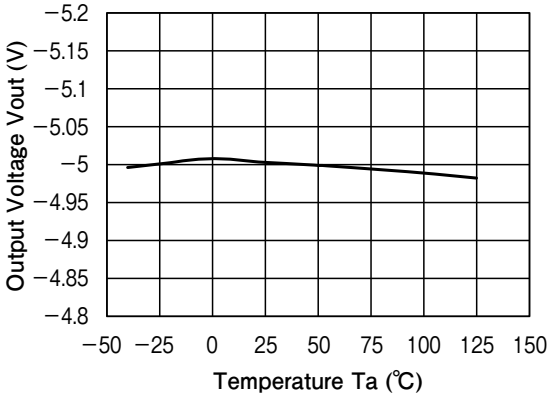
Load regulation



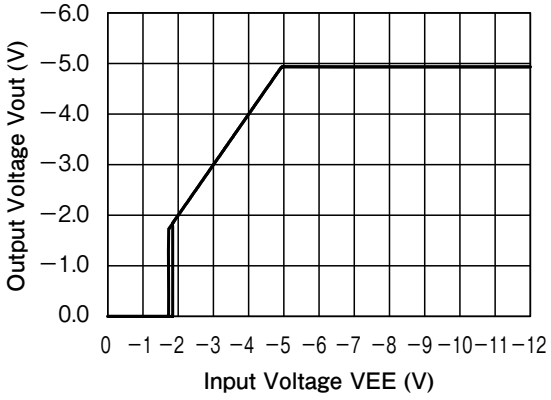
Line regulation



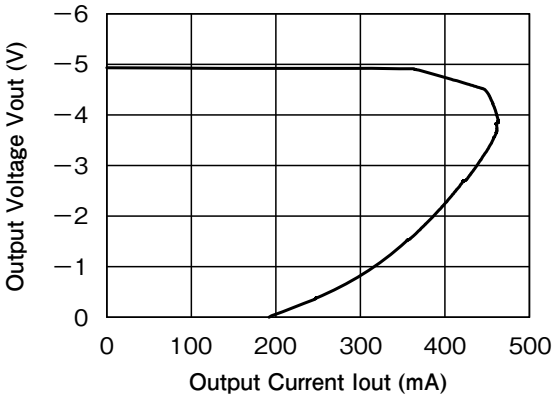
Output Voltage Temperature Coefficient



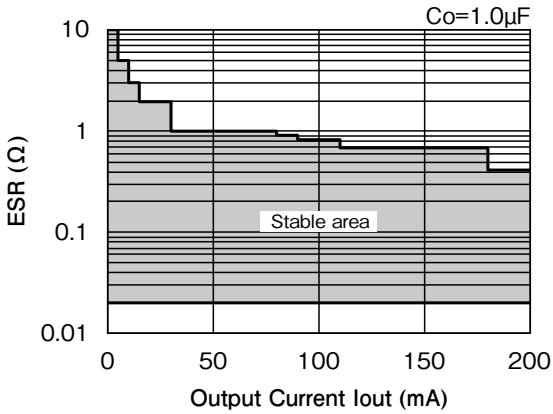
Input voltage − Output voltage



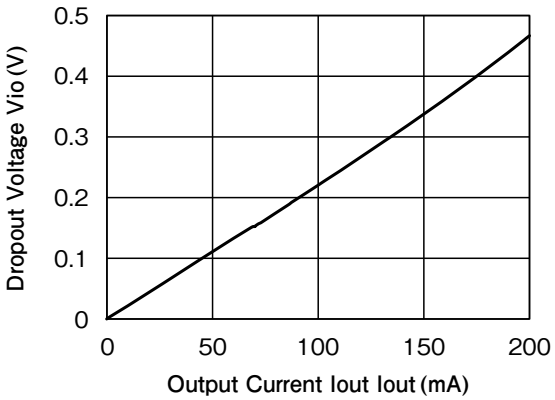
Output current – Output voltage



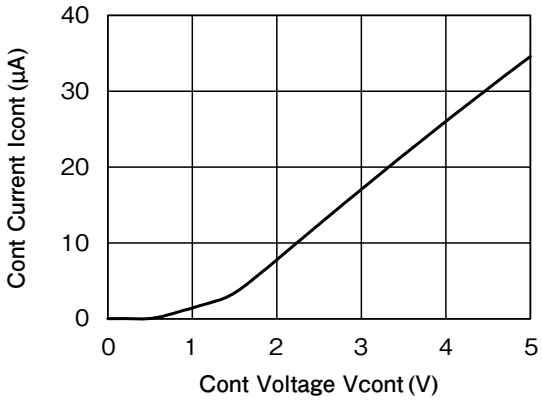
ESR stable area



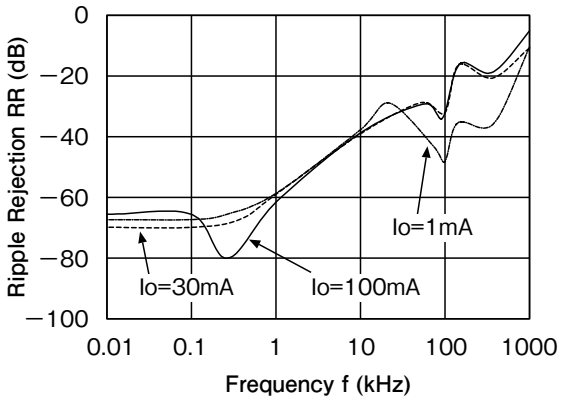
Output current – Dropout voltage



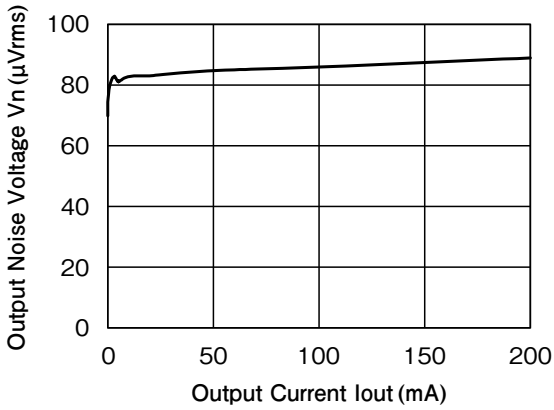
Cont voltage – Cont current



Ripple Rejection

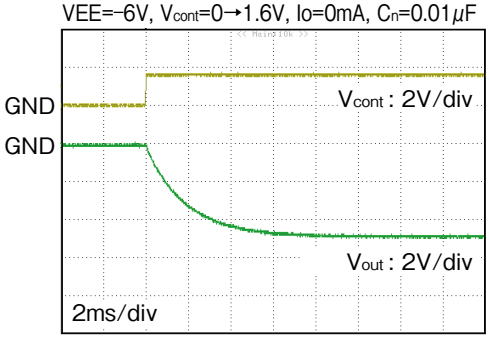


Cont voltage – Cont current

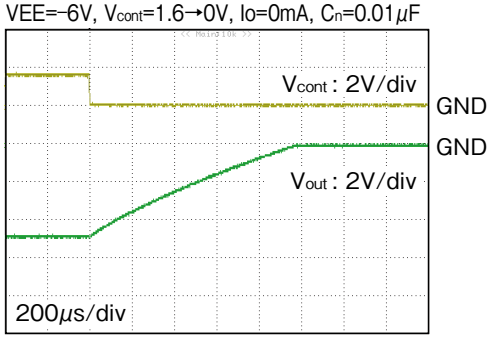


Cont rise characteristics

VEE=−6V, V_{cont}=0→1.6V, Io=0mA, C_n=0.01μF

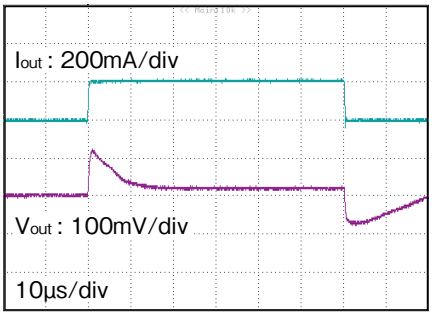


VEE=−6V, V_{cont}=1.6→0V, Io=0mA, C_n=0.01μF



Load transient characteristics

I_{out}=0.1mA⇔200mA



I_{out}=10mA⇔50mA