4-7cells Li-ion/polymer battery protection IC

MM3877 series

Outline

The MM3787 series are protection IC using high voltage CMOS process for overcharge, overdischarge, overcurrent, temperature protection, and cell balance control of the rechargeable Lithium-ion or Lithium-polymer battery.
The overcharge, overdischarge, discharging overcurrent, charging overcurrent, and short of the rechargeable 4-7cells lithium-ion or lithium-polymer battery can detected. In addition, the temperature detection by external NTC thermistor and cell balance control are also possible. The internal circuit of IC is composed by the voltage detector, the reference voltage source, oscillator, counter circuit and the logical circuit, etc. A stacking configuration using multiple ICs is also possible, so a low-cost, space-saving protection circuit can be configured for applications with more than 7 cells.

Features

・Range and accuracy of detection/release voltage/temperature (Unless otherwise specified, Topr=+25°C)

	Range	Accuracy
Overcharge detection voltage	3.6V to 4.5V, 5mV step	±20mV
Overcharge release voltage *1	3.4V to 4.5V, 50mV step	±30mV
Overdischarge detection voltage	2.0V to 3.0V, 50mV step	±50mV
Overdischarge release voltage *2	2.0V to 3.5V, 50mV step	±100mV
Cell balance detection voltage	3.6V to 4.5V, 5mV step	±25mV
Discharging overcurrent detection voltage1	30mV to 300mV, 5mV step	±10% (Min.±5mV)
Discharging overcurrent detection voltage2	60mV to 600mV, 6mV step	±15% (Min.±15mV)
Short detection voltage	200mV to 1.0V, 50mV step	±20%
Charging overcurrent detection voltage	-300mV to -20mV, 5mV step	±10% (Min.±5mV)
High/low temp protection detection temperature *3	-40°C to 75°C , 5°C step	±5°C

・SEL pin can be set from 4cell protection to 7 cell protection.

・Power save function

After overdischarge detection, if the charger is not connected and any cell voltage is below the overdischarge release voltage and the power save delay time has elapsed, the IC enters power save mode.
In power save mode, the IC stops unnecessary circuits and reduces current consumption.

・Cascade connection

By cascading two ICs, it is possible to protect batteries of 8 cells or more.
By connecting the OV pin and DCHG pin of the high side IC to the SOC pin and SDC pin of the low side IC respectively, it is possible to transmit charge/discharge control signal from high side IC to low side IC and the charge/load connection signal from the low side IC to high side IC. Various functions can be supported without increasing the number of external circuits in cascade connection.

Features

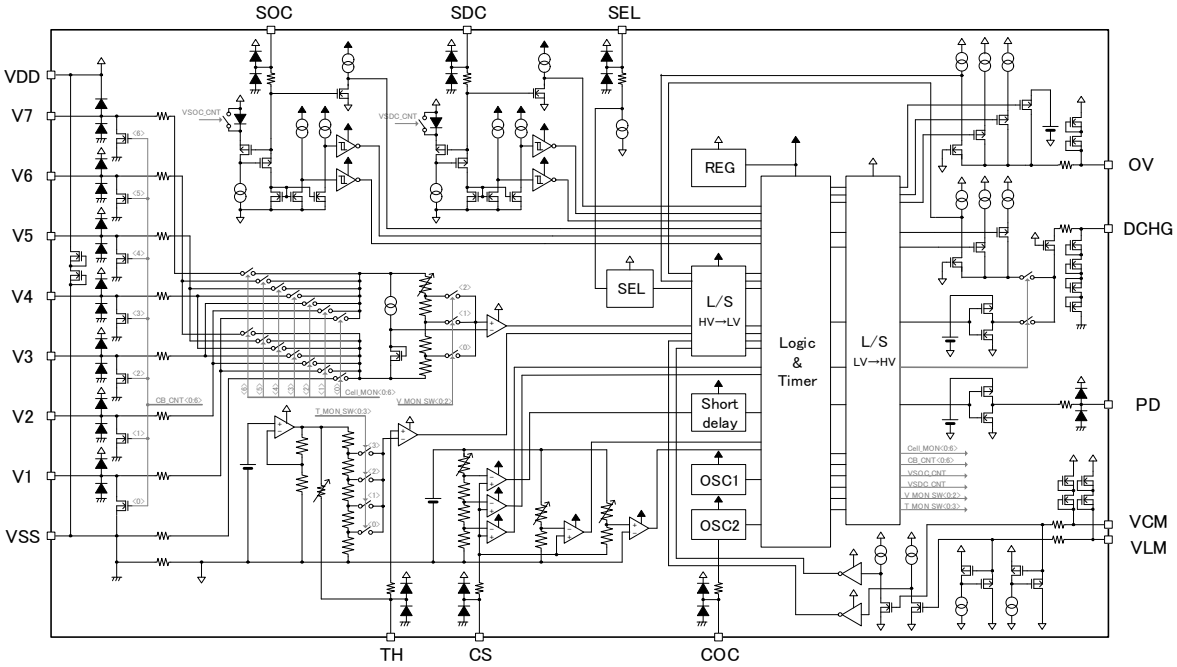
・0V battery charge function	Selection from "Permission" or " Inhibition"
・Current consumption	
Ave. current consumption (Normal mode)	Typ. 20.0uA Max. 30.0uA (VCELL=3.5V)
Current consumption (power save mode)	Typ. 1.0uA Max. 1.5uA (VCELL=1.8V)

*1 Overcharge release function is selectable from 2 options(voltage decrease, charger remove).
*2 Overdischarge release function is selectable from 2 options(voltage increase , load remove).
*3 High/Low temp protection detection temperature accuracy is guaranteed by design.
Detection accuracy may change with the specification of the used NTC thermistor.

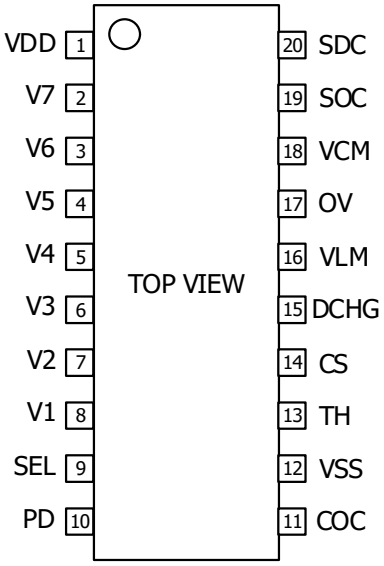
Package type

・VSOP-20A	8.66 × 6.00 × 1.50 [mm]

Block Diagram



Package



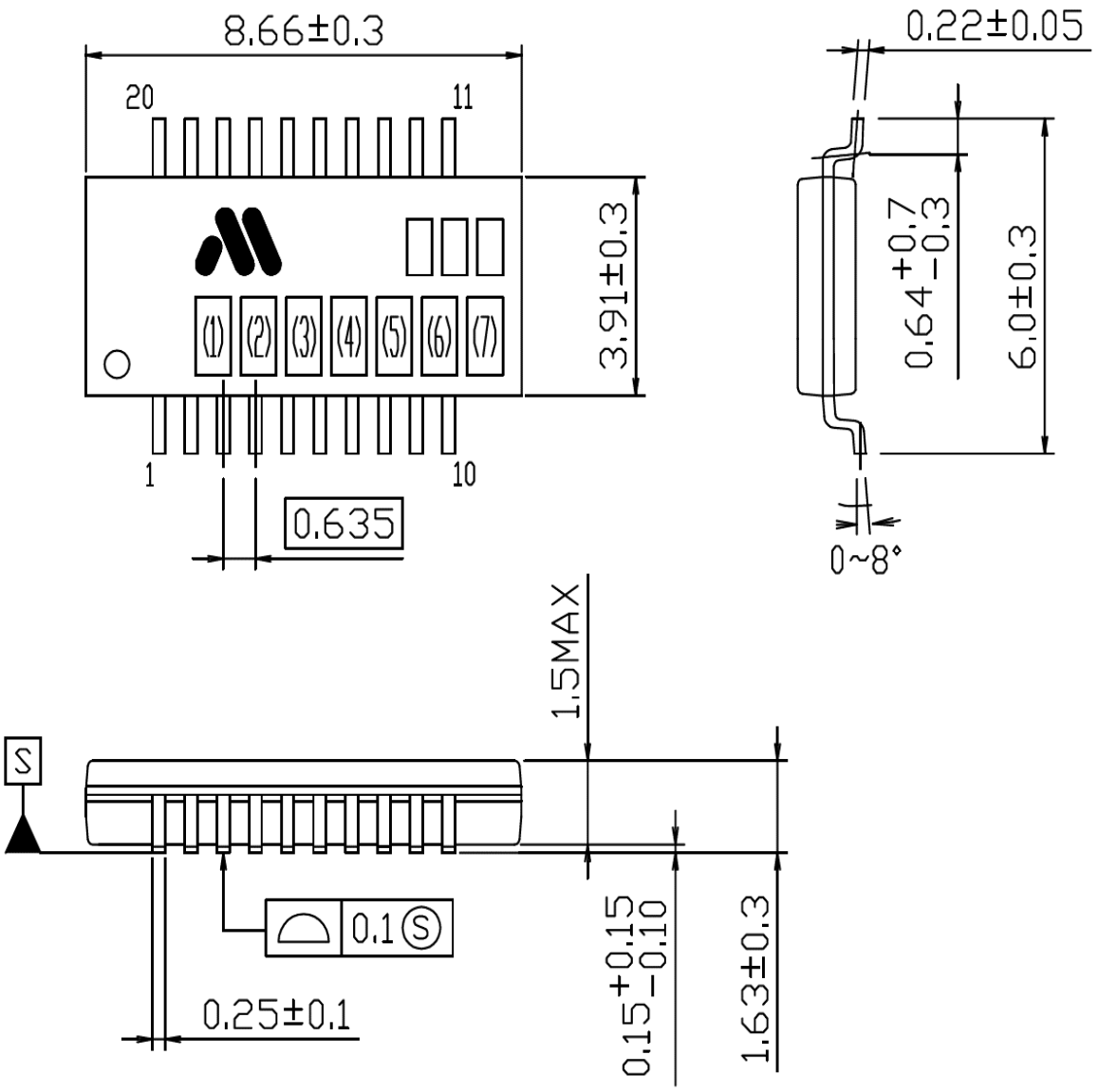
Pin configuration

PIN No.	Symbol	Function
1	VDD	The input pin of the power supply of IC.
2	V7	The input pin of the positive voltage of V7 cell and the output pin of cell balance control of V7 cell.
3	V6	The input pin of the positive voltage of V6, and the negative voltage of V7 cell. And the output pin of cell balance control of V6 cell.
4	V5	The input pin of the positive voltage of V5, and the negative voltage of V6 cell. And the output pin of cell balance control of V5 cell.
5	V4	The input pin of the positive voltage of V4, and the negative voltage of V5 cell. And the output pin of cell balance control of V4 cell.
6	V3	The input pin of the positive voltage of V3, and the negative voltage of V4 cell. And the output pin of cell balance control of V3 cell.
7	V2	The input pin of the positive voltage of V2, and the negative voltage of V3 cell. And the output pin of cell balance control of V2 cell.
8	V1	The input pin of the positive voltage of V1, and the negative voltage of V2 cell. And the output pin of cell balance control of V1 cell.
9	SEL	This input pin is changing function for 4cell, 5cell, 6cell, and 7cell in series. SEL=VDD : 7cell mode, SEL=V4 : 6cell mode, SEL=V2 : 5cell mode, SEL=VSS=4cell mode
10	PD	The output pin for controlling pull-down of load negative voltage.
11	COC	This input pin sets delay time of discharging overcurrent detection, and selects mode. It is able to set delay time by connecting a condenser between VSS pin and COC pin. Connect condenser between VSS : Charge/Discharge control FET drive mode COC=VDD : Cascade connection mode
12	VSS	The input pin of the negative voltage of V1 cell. The input pin the ground of IC.
13	TH	Temperature detection pin. Detected temperature by NTC thermistor between TH-VSS pins.
14	CS	The input pin of over current detection. Detected overcurrent by sense resistor between CS-VSS pins.
15	DCHG	When charge/discharge control FET drive mode, DCHG pin is discharge control output pin. When cascade mode, DCHG pin is discharge control output pin and load connect signal input pin. Charge/discharge control FET drive mode : Output type is CMOS. ・Normal state : VDCHG=High ・Discharge inhibition state : VDCHG=Low Cascade connection mode : Output type is constant current. ・Normal state : IDCHG=Typ.1.1uA ・Overdischarge state : IDCHG=0A ・Temp protection state : IDCHG=Typ.6.5uA
16	VLM	The input pin connected to load negative voltage. Detected load connection.
17	OV	When charge/discharge control FET drive mode, OV pin is charge control output pin. When cascade mode, OV pin is charge control output pin and charger connect signal input pin. Charge/discharge control FET drive mode : Output type is CMOS. ・Normal state : VOV =High ・Charge inhibition state : VOV=Hi-Z Cascade connection mode : Output type is constant current. ・Normal state : IOV=Typ.1.1uA ・Overcharge state : IOV=0A ・Temp protection state : IOV=Typ.6.5uA
18	VCM	The input pin connected to charger negative voltage. Detected charger connection.
19	SOC	The input pin for charge control. And, charger connect signal output pin.
20	SDC	The input pin for discharge control. And, load connect signal output pin.

Package dimensions

Unit:mm

VSOP-20A



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 to 42	V
V7 pin supply voltage	V7	VSS-0.3 to VDD+0.3	V
Voltage between cell input pins	VCELL	-0.3 to 6	V
SEL pin , COC pin input supply voltage	VSEL,VCOC	VSS-0.3 to VDD+0.3	V
PD pin supply voltage	VPD	VSS-0.3 to VDD+0.3	V
TH pin, CS pin supply voltage	VTH,VCS	VSS-0.3 to VDD+0.3	V
DCHG pin supply voltage	VDCHG	VDD-42 to VDD+10	V
OV pin supply voltage	VOV	VDD-42 to VDD+0.3	V
VLM pin, VCM pin supply voltage	VVLM,VVCM	VDD-42 to VDD+0.3	V
SOC pin, SDC pin supply voltage	VSOC,VSDC	VSS-0.3 to VDD+0.3	V
Storage temperature	Tstg	-55 to 125	degC
Power Dissipation	Pd	340	mW

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Operating ambient temperature	Topr	-40 to +85	degC
Operating voltage	Vop	3.5 to 31.5	V

Electrical characteristics

Unless otherwise specified, Topr=+25℃, VDD=24.5V, VCELLn=3.5V, RTH=10kΩ
SEL=VDD, CS=VLM=VCM=SOC=SDC=VSS, ROV=1MΩ

Parameter			Symbol	Conditions	Min.	Typ.	Max.	UNIT
Current consumption / Input current								
Ave. current consumption (Normal mode)			Idd	Vcell=3.5V	-	20.0	30.0	uA
Current consumption (Power save mode)			Idd_ps	Vcell=1.8V	-	1.0	1.5	uA
V7 pin input current (Normal mode)			Iv7	Vcell=3.5V	-	0.2	0.5	uA
V1-6 pin input current (Normal mode)			Ivn	Vcell=3.5V	-0.30	-	0.30	uA
V1-7 pin input current (Cell balance mode)			Ivn_cb	Vcell=4.5V	3.0	6.0	-	mA
Detection/Release voltage/temperature								
Overcharge detection voltage			Vovp		Typ-0.020	Vovp	Typ+0.020	V
Overcharge release voltage			Vovr		Typ-0.030	Vovr	Typ+0.030	V
Overdischarge detection voltage			Vuvp		Typ-0.050	Vuvp	Typ+0.050	V
Overdischarge release voltage			Vuvr		Typ-0.100	Vuvr	Typ+0.100	V
Cell balance detection voltage			Vcbd		Typ-0.025	Vcbd	Typ+0.025	V
Cell balance hysteresis voltage *5			Vcbh		Typ-0.005	Vcbh	Typ+0.005	V
Discharging overcurrent detection voltage 1			Vdocp1		Typ-10%	Vdocp1	Typ+10%	V
Discharging overcurrent detection voltage 2			Vdocp2		Typ-15%	Vdocp2	Typ+15%	V
Short detection voltage			VSCP		Typ-20%	Vscp	Typ+20%	V
Charging overcurrent detection voltage			Vcocp		Typ-10%	Vcocp	Typ+10%	V
VLM pin detection voltage			Vlm_d		1.50	2.00	2.50	V
VCM pin detection voltage			Vcm_d		-0.060	-0.030	0.000	V
CS pin detection voltage for discharging			Vld		1.5	3.0	4.5	mV
High temp protection	detection temp *5	for discharge control	Tthp1	RNTC=10kΩ±1%, B=3950±1%	Typ-5	Tthp1	Typ+5	℃
	release temp *5		Tthr1		Typ-5	Tthr1	Typ+5	℃
	detection temp *5	for charge control	Tthp2		Typ-5	Tthp2	Typ+5	℃
	release temp *5		Tthr2		Typ-5	Tthr2	Typ+5	℃
Low temp protection	detection temp *5	for discharge control	Tthp3		Typ-5	Tthp3	Typ+5	℃
	release temp *5		Tthr3		Typ-5	Tthr3	Typ+5	℃
	detection temp *5	for charge control	Tthp4		Typ-5	Tthp4	Typ+5	℃
	release temp *5		Tthr4		Typ-5	Tthr4	Typ+5	℃
Delay time								
Overcharge detection delay time			tovp		※6	tovp	※6	sec
Overdischarge detection delay time			tuvp		※6	tuvp	※6	sec
Cell balance detection delay time			tcbd		※6	tcbd	※6	msec
Discharging overcurrent detection delay time 1			tdocp1	COC=0.01uF	Typ-25%	tdocp1	Typ+25%	msec
Discharging overcurrent detection delay time 2			tdocp2	COC=0.01uF	Typ-25%	tdocp2	Typ+25%	msec
Short detection delay time			tscp		Typ-50%	tscp	Typ+50%	usec
Discharging overcurrent release delay time			tdocr		Typ-25%	tdocr	Typ+25%	msec
Charging overcurrent detection delay time			tcocp		Typ-25%	tcocp	Typ+25%	msec
Charging overcurrent release delay time			tcocr		Typ-25%	tcocr	Typ+25%	msec
Temp protection detection delay time			tthp		Typ-25%	tthp	Typ+25%	msec
Temp protection release delay time			tthr		Typ-25%	tthr	Typ+25%	msec
Temp protection monitoring time			tthm		12.0	16.0	20.0	msec
Temp protection monitoring period			ttmon		2.01	2.68	3.35	msec

*5 This parameter is guaranteed by design.

*6 Since the timing when the cell voltage changes and the timing when the cell voltage is monitored deviates, the delay time varies within the range of the spec.

Electrical characteristics

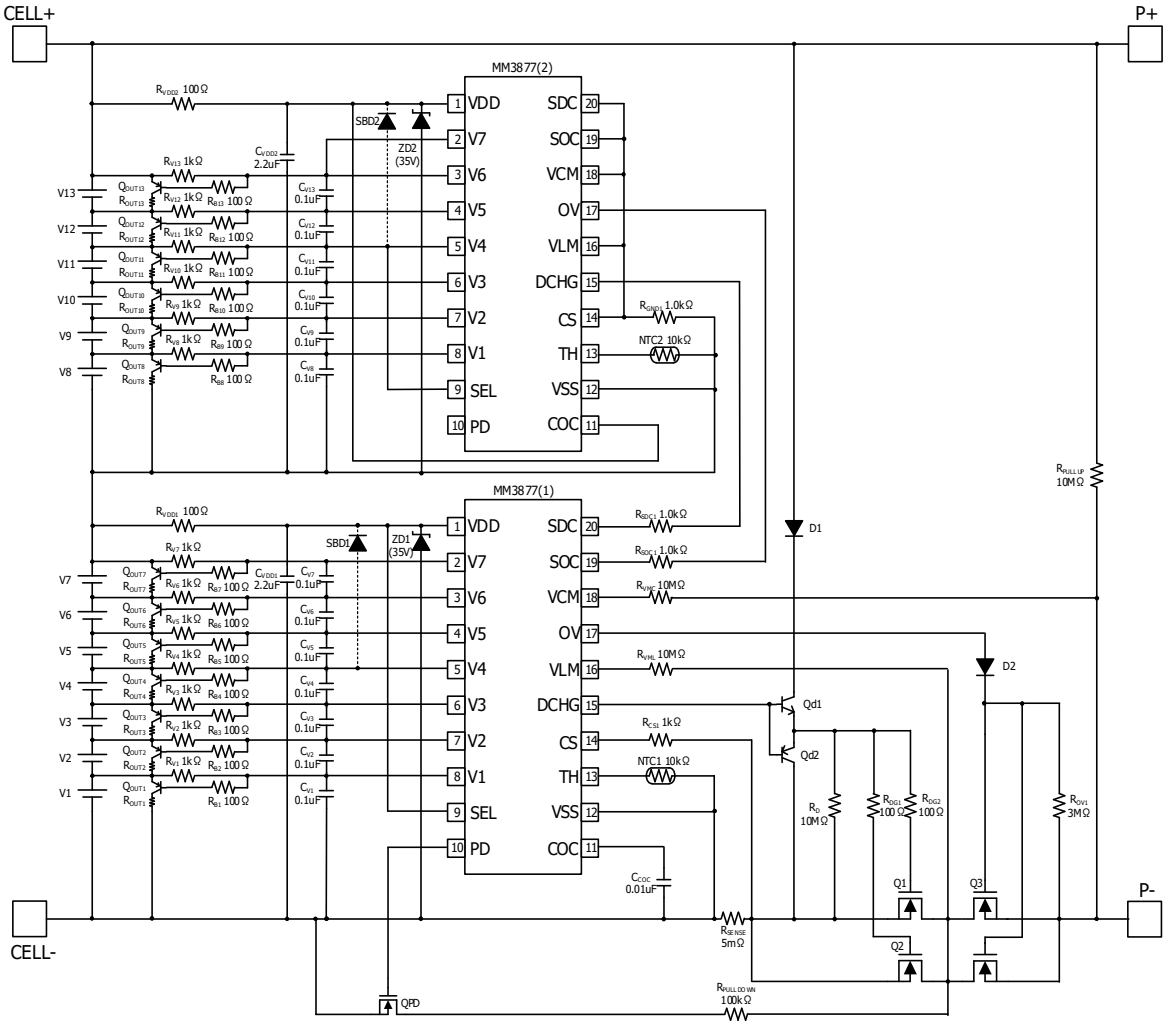
Unless otherwise specified, Topr=+25℃, VDD=24.5V, VCELLn=3.5V, RTH=10kΩ
SEL=VDD, CS=VLM=VCM=SOC=SDC=VSS, ROV=1MΩ

Parameter	Symbol	Conditions	Min.	Typ.	Max.	UNIT
Delay time						
Power save delay time	tps		1.536	2.048	2.560	sec
Power save release delay time	tpsr		1.50	2.00	2.50	msec
Output pin						
DCHG pin output voltage L	Vdchg_l	Idchg=200uA	-	0.50	0.80	V
DCHG pin output voltage H	Vdchg_h	Idchg=-200uA	12.0	14.5	17.5	V
DCHG pin output current L	Idchg_l	COC=VDD,DCHG=-1V	0.65	1.10	1.55	uA
DCHG pin output current H	Idchg_h	COC=VDD,DCHG=-1V	3.80	6.50	9.20	uA
DCHG pin leak current	Idchg_leak	COC=VDD,DCHG=-3V	-	-	0.1	uA
DCHG pin detection voltage	Vdchg_d		-1.70	-1.40	-1.10	V
OV pin output voltage H	Vov_h	Iov=-200uA	12.0	14.5	17.5	V
OV pin output current L	Iov_l	COC=VDD,OV=-1V	0.65	1.10	1.55	V
OV pin output current H	Iov_h	COC=VDD,OV=-1V	3.80	6.50	9.20	uA
OV pin leak current	Iov_leak	COC=VDD,OV=-3V	-	-	0.1	uA
OV pin detection voltage	Vov_d		-1.70	-1.40	-1.10	V
PD pin output voltage L	Vpd_l	Ipd=200uA	-	0.50	0.80	V
PD pin output voltage H	Vpd_h	Ipd=-200uA	12.0	14.5	17.5	V
Others						
Cell voltage monitoring period	tvmon		-	71.75	-	msec
Cell voltage monitor detection delay time	tvd		-	32.00	-	msec
Cell voltage monitor release delay time	tvr		-	8.00	-	msec
SDC detection current L	Isdc_l		0.20	0.40	0.55	uA
SDC detection current H	Isdc_h		1.65	2.70	3.70	uA
SDC output voltage L	Vsdc_l		VDD-4.10	VDD-3.30	VDD-2.50	V
SDC output voltage H	Vsdc_h		VDD-0.80	VDD-0.60	VDD-0.40	V
SDC detection delay time	tsdcd		1.50	2.00	2.50	msec
SDC release delay time	tsdcr		3.00	4.00	5.00	msec
SDC enable voltage	Vsdc_en		-	-	0.30	V
SOC detection current L	Isoc_L		0.20	0.40	0.55	uA
SOC detection current H	Isoc_h		1.65	2.70	3.70	uA
SOC output voltage L	Vsoc_l		VDD-4.10	VDD-3.30	VDD-2.50	V
SOC output voltage H	Vsoc_h		VDD-0.80	VDD-0.60	VDD-0.40	V
SOC detection delay time	tsocd		1.50	2.00	2.50	msec
SOC release delay time	tsocr		3.00	4.00	5.00	msec
SOC enable voltage	Vsoc_en		-	-	0.30	V
SEL pin input voltage (4S mode)	Vsel_4s		-	-	0.50	V
SEL pin input voltage (5S mode)	Vsel_5s		0.50	-	V2+0.50	V
SEL pin input voltage (6S mode)	Vsel_6s		V2+0.50	-	VDD-0.50	V
SEL pin input voltage (7S mode)	Vsel_7s		VDD-0.50	-	-	V
SEL pin input current	Isel	SEL=VSS	-0.40	-0.20	-	uA
COC pin input voltage H	Voc_h		VDD-0.50	-	-	V
Recharge prohibited voltage	Vnorc		0.70	1.00	1.30	V

*7 This parameter stipulates each CELL voltage for which charging is prohibited when "0V charging is prohibited".

Typical application circuit

1) 13cells protection circuit (Current pathway : common)



These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied. Mitsumi Electric Co., Ltd. Assumes no responsibility for any trouble or damage as a result of the use of these circuits.

Typical application circuit

2) Explanation of external parts : 13cells protection circuit

Parts name	Roles of parts
R_{VDD1},RV_{DD2},R_{V1}-R_{V13}	CR low-pass filter to stabilize a supply ripple of VDD pin, V1 to V7 pins.
C_{VDD1},C_{VDD2},C_{V1}-C_{V13}	This resistor is used to drive an external pnp transistor during cell balance control.
ZD1,ZD2	Zener diode to prevent destruction of IC by surge voltage and motor back electromotive voltage.
SBD1,SBD2	This is a Schottky barrier diode to prevent the V4 pin voltage from exceeding VDD.
R_{B1}-R_{B13}	This resistor is the base resistor of the pnp transistor for cell balance control.
R_{OUT1}-R_{OUT13}	This resistor is the discharge resistor curing cell balance control.
Q_{OUT1}-Q_{OUT13}	PNP transistor for cell balance control.
R_{CS1},R_{VCM},R_{VLM},R_{SOC},R_{SDC},R_{GND1}	Resistor to protect terminal.
Q_{PD}	Nch MOS FET that controls the pull-down resistor when monitoring the load connection.
$R_{PULLDOWN}$	This is pull-down resistor for monitoring the load connection.
R_{SENSE}	Sense resistor to monitor charging/discharging current.
C_{COC}	Capacitor to sets discharging overcurrent detection delay time.
NTC1,NTC2	NTC thermistor to monitor to temperature.
Q_{DG1},Q_{DG2},R_D,D1	Parts for driving the discharge control FET.
R_{OV1}	Pull-down resistor to turn off the charge control FET.
R_{DG1},R_{DG2}	Resistors for preventing the gate destruction due to parasitic oscillation.
D2	This diode prevents current from flowing back to the OV pin.
Q1,Q2	Nch MOS FET to control discharging current.
Q3,Q4	Nch MOS FET to control charging current.
R_{PULLUP}	This is pull-up resistor for monitoring the charger connection.

3) Instructions and directions for use

- When the current pathway of charge and the discharge is separated, wiring is separated from the drain of charge and discharge control FET.
- If temperature protection function is repealed, make TH pin and VDD pin connection.
- IC, $Q_{OUT1-13}$, and $R_{OUT1-13}$ may generate heat during cell balance operation.
  It is recommended to layout the VIA for heat radiation is the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate).
  By increasing these copper foil pattern area of PCB, power dissipation improves.
- R_{VCM} and R_{VLM} each have high impedance, so place them close to the VCM and VLM pins.
- Lay the wiring between OV and SOC, between DCHG and SDC so that parasitic capacitance is as small as possible with other wiring.
- The temperature detection accuracy is the specification when using a thermistor with the following characteristics. In order to satisfy the characteristic of specification, it recommends using the following parts.

Symbol	Name	Function	Part name	Remarks
NTC1 NTC2	NTC Thermistor	10KΩ±1% B(25/50)=3950±1%	-	-

○NTC resistance

・Ra = R0 * exp (B * (1 / Ta - 1 / T0))

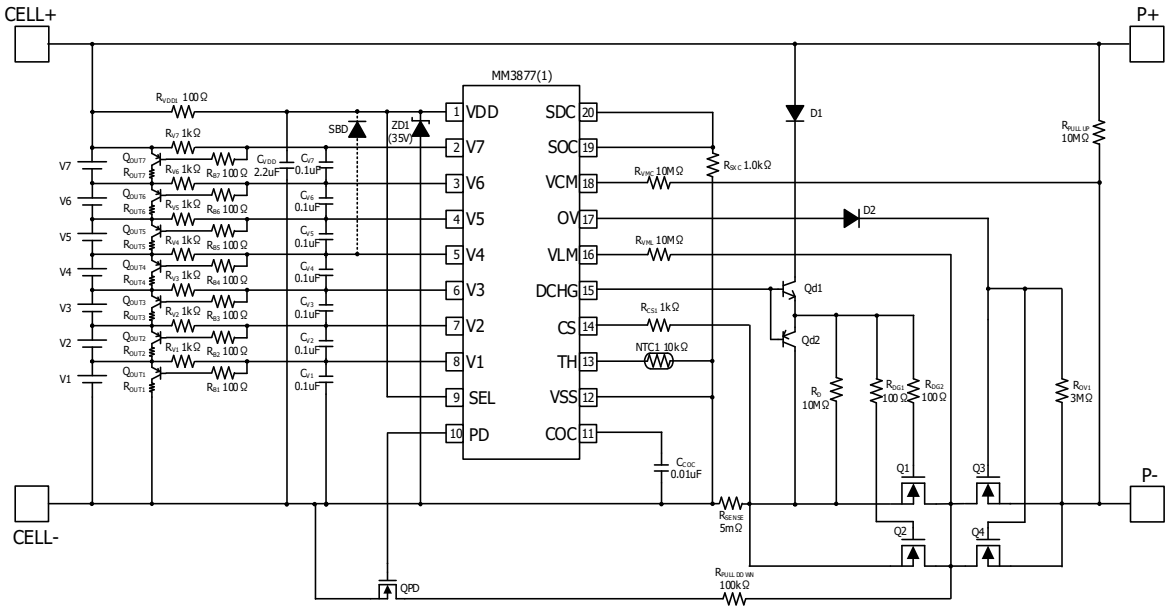
Ra : NTC resistance value at ambient temperature Ta(K).

R0 : NTC resistance value at ambient temperature T0(K).

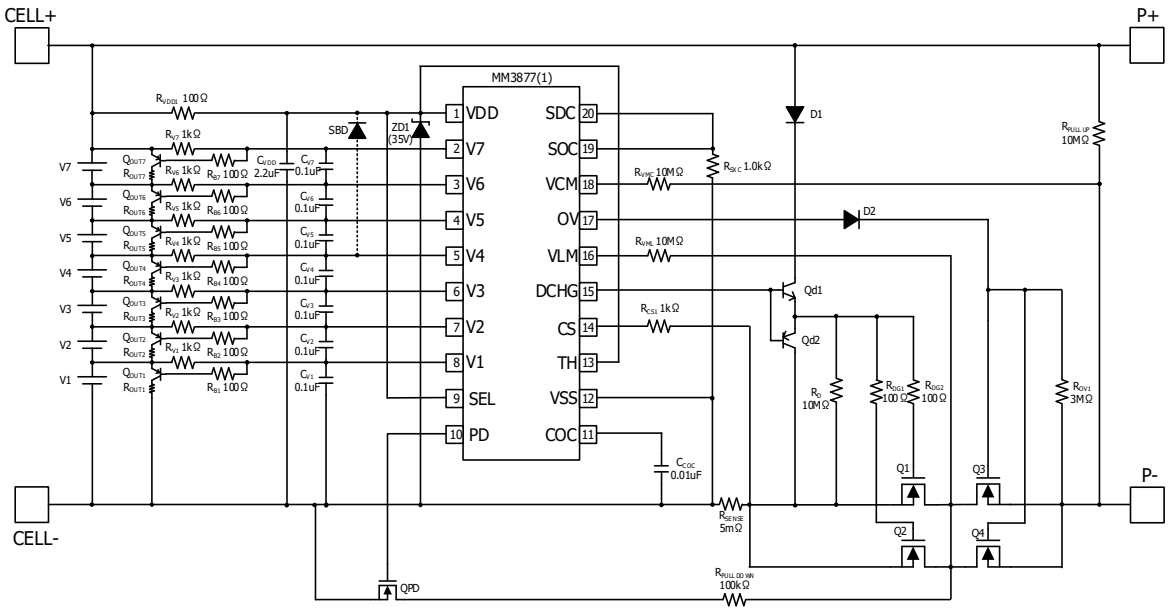
B : B constant of thermistor

Typical application circuit

4) 7cells protection circuit



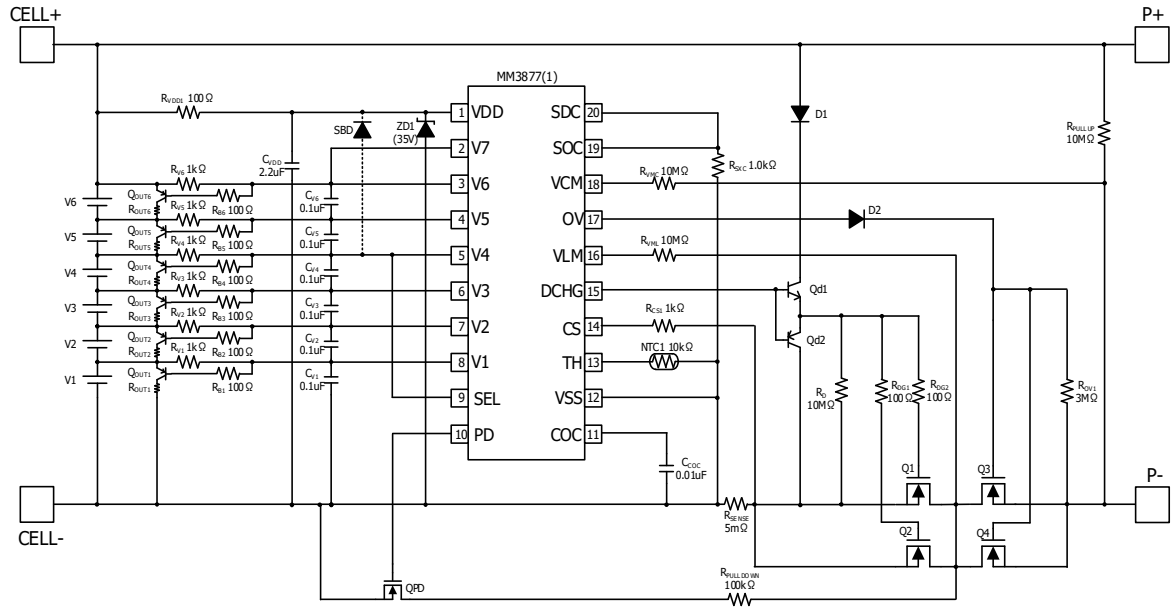
5) 7cells protection circuit (Temp protection disable)



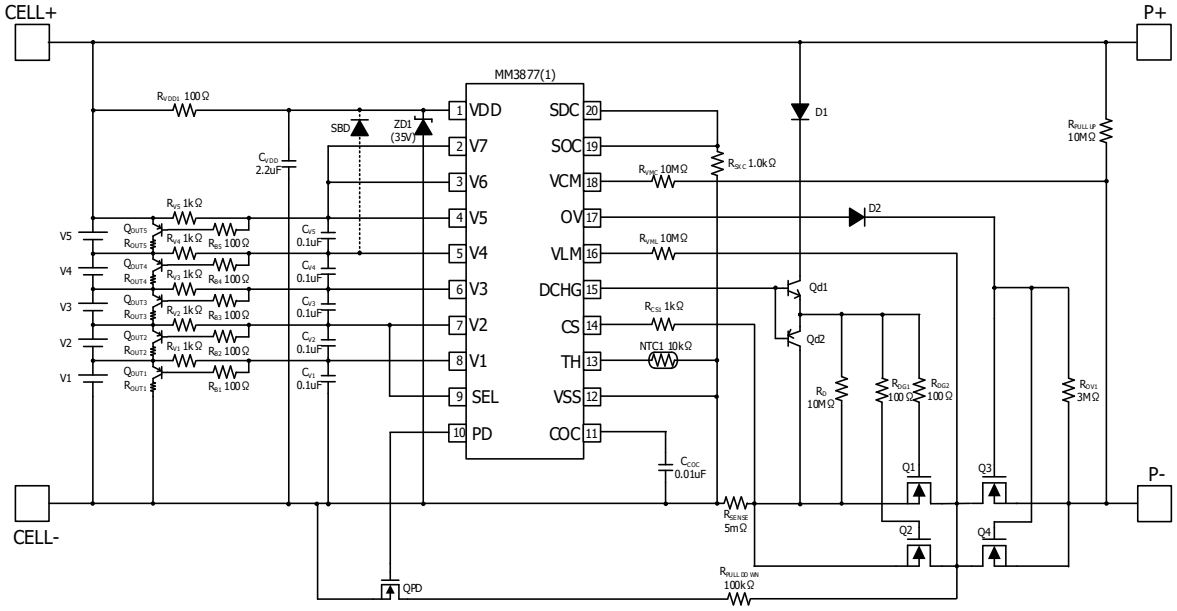
These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied. Mitsumi Electric Co., Ltd. Assumes no responsibility for any trouble or damage as a result of the use of these circuits.

Typical application circuit

6) 6cells protection circuit



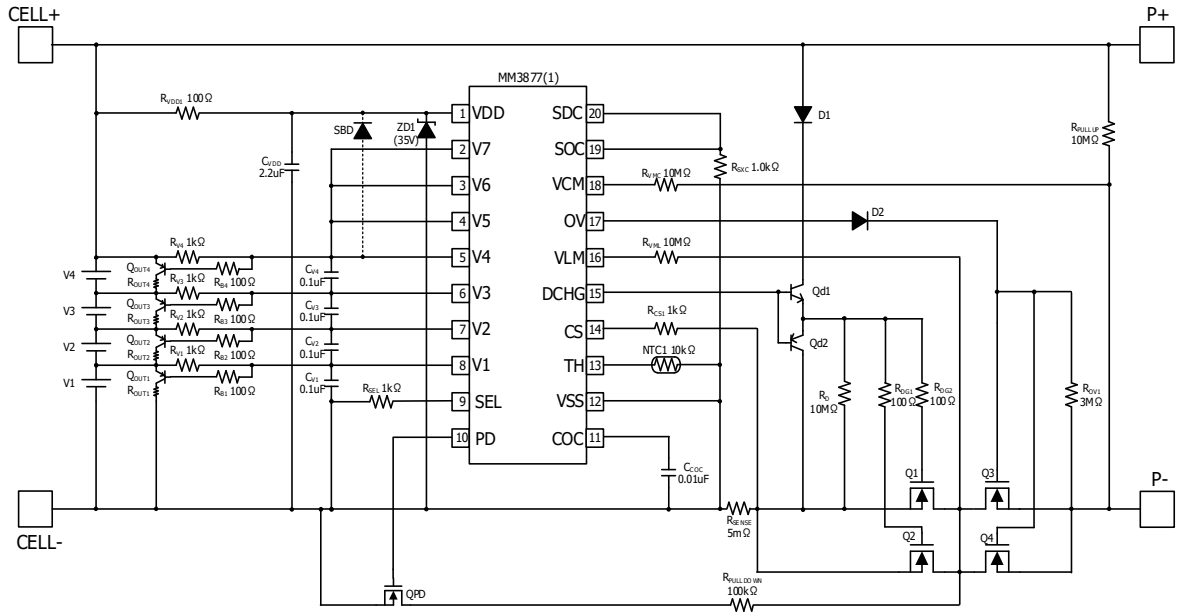
7) 5cells protection circuit



These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied. Mitsumi Electric Co., Ltd. Assumes no responsibility for any trouble or damage as a result of the use of these circuits.

Typical application circuit

8) 4cells protection circuit

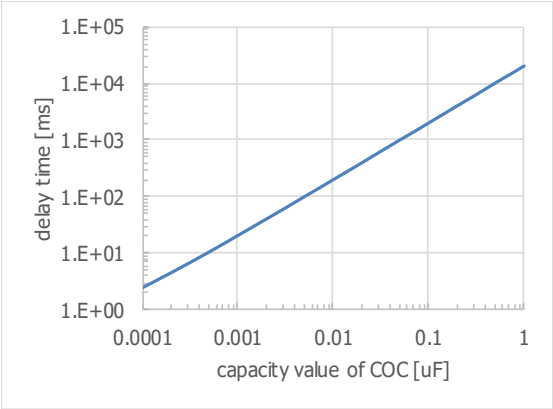


These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied. Mitsumi Electric Co., Ltd. Assumes no responsibility for any trouble or damage as a result of the use of these circuits.

Delay time characteristic

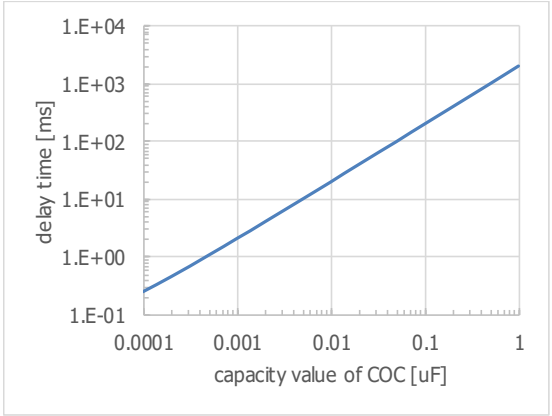
Discharging overcurrent detection delay time 1,2 are set by capacity connected to COC-VSS pins. The figure below shows typical characteristics of MM3877C02WBE. Since it is not a compensation value, please refer to it as reference data.

Discharging overcurrent detection delay time 1



delay time[msec] = tdocp1 / 10^-8 * COC

Discharging overcurrent detection delay time 2



delay time[msec] = tdocp2 / 10^-8 * COC

Lineup

Product name (MM3877***WBE)	Detection voltage / Release voltage									
	Overcharge detection voltage	Overcharge release voltage	Overdischarge detection voltage	Overdischarge release voltage	Cell balance detection voltage	Cell balance hysteresis voltage	Discharging overcurrent detection voltage 1	Discharging overcurrent detection voltage 2	Short detection voltage	Charging overcurrent detection voltage
	Vovp	Vovr	Vuvp	Vuvr	Vcbd	Vcbr	Vdocp1	Vdocp2	Vscp	Vcocp
	V	V	V	V	V	V	V	V	V	V
C05	4.250	4.100	2.750	3.000	4.200	0.010	0.100	0.200	0.350	-0.030

Product name (MM3877***WBE)	Temperature protection detection / release temperature									
	High temp protection detection temperature for	High temp protection release temperature for discharging	High temp protection detection temperature for	High temp protection release temperature for charging	Low temp protection detection temperature for	Low temp protection release temperature for charging	Low temp protection detection temperature for	Low temp protection release temperature for discharging	Temp protection monitoring time	Temp protection monitoring period
	Tthp1	Tthr1	Tthp2	Tthr2	Tthp3	Tthr3	Tthp4	Tthr4	tthm	ttmon
	℃	℃	℃	℃	℃	℃	℃	℃	msec	sec
C05	75	65	50	40	0	10	-	-	16.0	2.68

Product name (MM3877***VBH)	Detection delay time / Release delay time										
	Overcharge detection delay time	Overdischarge detection delay time	Cell balance detection delay time	Discharging overcurrent detection delay time 1 (at COC = 0.01uF)	Discharging overcurrent detection delay time 2 (at COC = 0.01uF)	Discharging overcurrent release delay time	Short detection delay time	Changing overcurrent detection delay time	Charging overcurrent release delay time	Temp protection detection delay time	Temp protection release delay time
	tovp	tuvp	tcbd	tdocp1	tdocp2	tdocr	tscp	tcocp	tcocr	tthp	tthr
	sec	sec	sec	msec	msec	msec	usec	msec	msec	sec	msec
C05	1.024	1.024	0.256	100	10	1024	350	1024	128	2.048	100

Lineup

Product name (MM3877***VBH)	Option function							
	Cell balance function	Overcharge release function *8	Overdischarge hysteresis cancel function	Overdischarge release function *9	Discharging overcurrent release function	Charging overcurrent release function	Temp protection release function	0V battery charge function
C05	Enable	Latch	Enable	Latch	Load remove	Charger remove	Temp	Prohibition

*8 In the “Latch” type, IC release overcharge state by remove charger and by all cell voltages are less than or equal to the overcharge release voltage.

*9 In the “Latch” type, IC release overdischarge state by remove load and by all cell voltages are more than or equal to the overdischarge release voltage.