3 to 5cells Li-ion/Li-polymer battery protection IC
MM3575 Series

Outline

The MM3575 series are protection IC using high voltage CMOS process for overcharge, overdischarge and overcurrent protection of the rechargeable Lithium-ion or Lithium-polymer battery. The overcharge, overdischarge, discharging overcurrent, charging overcurrent, cell balance and V5 to V3 pin disconnect of the rechargeable 3 to 5cell Lithium-ion or Lithium-polymer battery can be detected. By using cascade connection, it is also possible to protect 6 or more cells rechargeable Lithium-ion battery. And the regulator can be constructed by using external Nch MOS FET. The internal circuit of IC is composed by the voltage detector, the reference voltage source, delay time control circuit, and the logical circuit, etc.

Features (Unless otherwise specified, Topr=+25°C)

(1) Range and accuracy of detection/release voltage

●Overcharge detection voltage	3.6V to 4.5V, 5mV steps	Accuracy±25mV (Topr=±0 to +50°C)
●Overcharge release voltage	3.4V to 4.5V, 50mV steps	Accuracy±50mV
●Overdischarge detection voltage	2.0V to 3.0V, 50mV steps	Accuracy±80mV
●Overdischarge release voltage (Note4)	2.0V to 3.0V, 50mV steps	Accuracy±100mV
●Discharging overcurrent detection voltage 1	30mV to 300mV, 5mV steps	Accuracy±15mV (typ 50mV~)
●Discharging overcurrent detection voltage 2	Twice or 4 times of discharging overcurrent 1 (Note1)	Accuracy±15%
●Short detection voltage	4 or 8 times of discharging overcurrent 1 (Note1)	Accuracy±100mV
●Charging overcurrent detect voltage	–300mV to –20mV, 5mV steps	Accuracy±10mV
●Cell balance detection voltage	3.6V to 4.5V, 5mV steps	Accuracy±30mV (Topr=±0 to +50°C)

(2) Range of detection delay time

●Overcharge detection delay time	Selection from 0.25s, 1.0s, 1.2s, 4.1s	Accuracy±25%
●Overcharge release delay time	Selection from 10ms, 24ms, 48ms, 100ms	Accuracy±25%
●Overdischarge detection delay time	Selection from 0.25s, 1.0s, 1.2s, 4.1s	Accuracy±25%
●Overdischarge release delay time	Selection from 4ms, 8ms, 12ms, 24ms	Accuracy±25%
●Discharging overcurrent detection delay time1	Setting by a capacitor of COC pin. (Note2)	Accuracy±30%
●Discharging overcurrent detection delay time2	Setting by a capacitor of COC pin. (Note2)	Accuracy±30%
●Short detection delay time	Selection from 100μs, 200μs, 300μs	Accuracy±50%
●Discharging overcurrent release delay time	Setting by a capacitor of COC pin. (Note2)	Accuracy±30%
●Charging overcurrent detection delay time	Setting by a capacitor of COC pin. (Note2)	Accuracy±30%
●Charging overcurrent release delay time	Setting by a capacitor of COC pin. (Note2)	Accuracy±30%
●Disconnect detection delay time	Selection from 25ms, 50ms, 100ms	Accuracy±25%
●Disconnect release delay time	Selection from 1024ms, 2048ms, 4096ms	Accuracy±25%
●Cell balance detection delay time	Selection from 0.1s, 0.25s, 0.5s (Note3)	Accuracy±25%
●Cell balance release delay time	Selection from 4ms, 8ms, 12ms	Accuracy±25%

Note1 : Optional function

Note2 : Since the capacity is the same, each delay times will change when a value is changed without short detection delay time.

Note3 : Cannot do shorter than disconnect detection delay time.

Note4 : The discharge state release method can choose a voltage release and a load open.

(3) Protected operation can be detectof V5~V1 pin disconnection

When any of V5 to V1 pin open, it will detect disconnection and charge and discharge prohibited state.
Protection mode of disconnection can be chosen from three, prohibition of charge, prohibition of discharge and prohibition of charge and discharge (Optional)
The release from disconnection protection is done by disconnection point being connected.

(4) The setting for three cell, for four cell, and for five cell protection can be set with the SEL pin.

(5) The charge and discharge of the battery can be controlled with SDC pin and SOC pin.

(6) 0V battery charge function Selection from "Prohibition" or "Permission"

(7) Power save mode built-in

It is possible to make it shift to low consumption current mode arbitrarily.
Transition of power save mode is used by SDC,SOC pins.
It shifts to a power save mode by making SDC and SOC pin into a VSS level.

(8) Regulator function built-in

Connecting drain of external Nch MOS FET gate to DRIVE pin and source to REG_IN pin, it can operate as a regulator.
The regulator operates independently with protected operation, such as overcharge detection.
Regulator voltage can be chosen at 0.1V step among 3.3V to 5.0V.

(9) Low current consumption

●VDD pin current consumption (Vcell=4.3V)	Typ. 25.0μA, Max. 35.0μA
●VDD pin current consumption (Vcell=3.5V)	Typ. 20.0μA, Max. 30.0μA
●VDD pin current consumption (Vcell=2.0V)	Typ. 10.0μA, Max. 15.0μA
●VDD pin current consumption at power save1 (Vcell=3.5V)	Typ. 12.0μA, Max. 16.0μA
●VDD pin current consumption at power save2 (Vcell=3.5V)	Typ. 4.0μA, Max. 6.0μA
●V5 pin current consumption (Vcell=4.3V)	Typ. 4.0μA, Max. 6.0μA
●V5 pin current consumption (Vcell=3.5V)	Typ. 2.0μA, Max. 3.0μA
●V5 pin current consumption (Vcell=2.0V)	Typ. 1.0μA, Max. 1.5μA
●V5 pin current consumption at power save (Vcell=3.5V)	Max. 0.05μA

(10) Input current

●V4 pin input current (Vcell=3.5V)	Max. 1.0μA
●V3 pin input current (Vcell=3.5V)	Max. 1.0μA
●V2 pin input current (Vcell=3.5V)	Max. 1.0μA
●V1 pin input current (Vcell=3.5V)	Max. 1.0μA

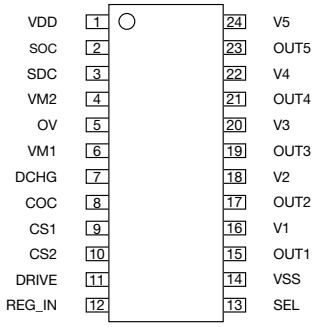
(11) Absolute maximum ratings

●VDD, CS1, CS2 pin	VSS−0.3V to VSS+30V
●V5 pin	V4−0.3V to VDD+0.3V
●Voltage between the input terminals	−0.3V to +10V
●OV, VM1, VM2 pin	VDD−30V to VDD+0.3V
●OUT1 to 5 pin	V_{n-1}−0.3V to VDD+0.3V
●DCHG, SEL, SDC, SOC pin	VSS−0.3V to VDD+0.3V
●DRIVE, REG_IN pin	VSS−0.3V to VDD+0.3V
●Storage temperature	−55 to +125°C

(12) Recommended operating conditions

●Operation temperature	−40 to +85°C
●Supply Voltage	VSS+3.5V to +22.5V

Pin Assignment

Top view VSOP-24A	Pin No.	Function
	1	The input terminal of the power supply of IC.
	2	The control terminal of output over charge detection. ISOC<ISOCL → OV=High impedance
	3	The control terminal of output over discharge detection. ISDC<ISDCL → DCHG=Low
	4	Input terminal connected to charger negative voltage. Detected charger connection.
	5	Charge control output terminal. Output type is Pch open drain. Normal mode → "High" Overcharge mode → "High impedance"
	6	Input terminal connected to discharge voltage. Detected load connection.
	7	Discharge control output terminal. Output type is CMOS. Normal mode → "High" Overdischarge mode → "Low"
	8	A terminal which sets delay time of discharging overcurrent and charging overcurrent detection/release. It is able to set delay time by connecting a condenser between VDD and COC terminals.
	9	Input of overcurrent detection. Detected overcurrent by sense resistor between CS1 pin and CS2 pin. And then the DCHG terminal outputs low level, and it protects from large current discharging.
	10	Common terminal of overcurrent detection circuit.
	11	The drive terminal of FET for regulator. Connect to gate of FET
	12	The input terminal of regulator voltage. Connect to source of FET
	13	This pin is for changing function for 3cell in series or 4cell in series , 5cell in series. Connect VSS→5cells in series Connect V2→4cells in series Connect VDD→3cells in series
	14	The input terminal of the negative voltage of V1 cell. The input terminal of the ground of IC.
	15	V1 cell balance control output terminal. Output type is CMOS. Normal mode → "Low" Cell balance detect mode → "High"
	16	The input terminal of the positive voltage of V1 cell, and the negative voltage of V2 cell.
	17	V2 cell balance control output terminal. Output type is CMOS. Normal mode → "Low" Cell balance detect mode → "High"
	18	The input terminal of the positive voltage of V2 cell, and the negative voltage of V3 cell.
	19	V3 cell balance control output terminal. Output type is CMOS. Normal mode → "Low" Cell balance detect mode → "High"
	20	The input terminal of the positive voltage of V3 cell, and the negative voltage of V4 cell.
	21	V4 cell balance control output terminal. Output type is CMOS. Normal mode → "Low" Cell balance detect mode → "High"
	22	The input terminal of the positive voltage of V4 cell, and the negative voltage of V5 cell.
	23	V5 cell balance control output terminal. Output type is CMOS. Normal mode → "Low" Cell balance detect mode → "High"
	24	The input terminal of the positive voltage of V5 cell.

Selection Guide

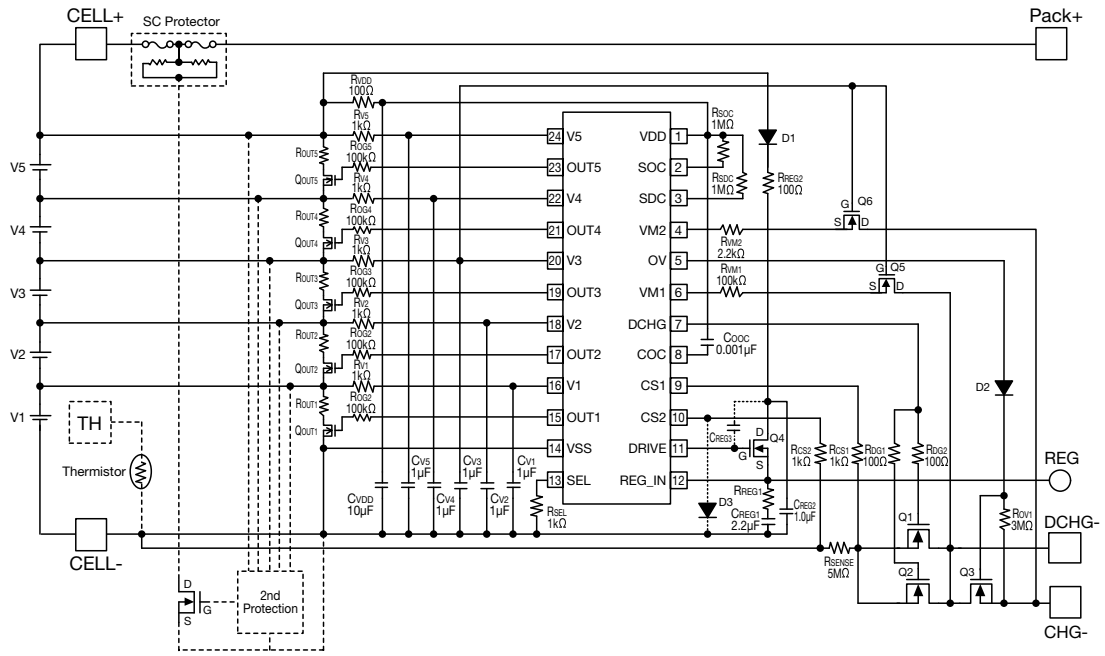
Product name (MM3575***WBH)	Detection voltage /Release voltage									0V battery charge function	Protection mode of disconnection
	Overcharge detection voltage [V]	Overcharge release voltage [V]	Overdischarge detection voltage[V]	Overdischarge release voltage [V]	Discharging overcurrent detection voltage 1 [V]	Discharging overcurrent detection voltage 2 [V]	Short detection voltage [V]	Charging overcurrent detection voltage [mV]	Cell balance detection voltage [mV]		
	V_{DET1}	V_{REL1}	V_{DET2}	V_{REL2}	V_{DET3-1}	V_{DET3-2}	V_{SHORT}	V_{DET4}	V_{DET_CB}		
MM3575A02WBH	4.250	4.175	2.800	2.900	0.100	0.200	0.400	–0.020	4.180	Prohibition	Prohibition of charge and discharge
MM3575A08WBH	4.250	4.100	2.600	3.200	0.090	0.180	0.360	–0.030	4.180	Prohibition	Prohibition of charge and discharge

Product name (MM3575***WBH)	Detection / Release delay time													
	Overcharge detection delay time [sec]	Overcharge release delay time [msec]	Overdischarge detection delay time [sec]	Overdischarge release delay time [msec]	Discharging overcurrent detection delay time 1 [msec]	Discharging overcurrent detection delay time 2 [msec]	Discharging overcurrent release delay time [msec]	Short detection delay time [usec]	Charging overcurrent detection delay time [msec]	Charging overcurrent release delay time [msec]	Disconnect detection delay time [msec]	Disconnect release delay time [msec]	Cell balance detection delay time [msec]	Cell balance release delay time [msec]
	t_{VDET1}	t_{VREL1}	t_{VDET2}	t_{VREL2}	$t_{VDET3-1}$	$t_{VDET3-2}$	t_{VREL3}	t_{SHORT}	t_{VDET4}	t_{VREL4}	t_{VDET5}	t_{VREL5}	$t_{VDET\ CB}$	t_{VREL_CB}
MM3575A02WBH	1.0	100	1.0	4.0	10.0	2.0	4.0	200	1024	128	200	4096	256	8.0
MM3575A08WBH	1.0	100	2.0	4.0	1536	60.0	4.0	200	100	128	200	4096	256	8.0

Please inquire to us, if you request a rank other than the above.

Application Circuit

· 5 cells protection circuit.



Explanation of external parts

Parts name	Roles of parts
R_{VDD} · R_{V5} · R_{V4} · R_{V3} · R_{V2} · R_{V1}	CR low-pass filter to stabilize a supply ripple of VDD pin · V5pin · V4pin · V3pin · V2pin · V1pin.
C_{VDD} · C_{V5} · C_{V4} · C_{V3} · C_{V2} · C_{V1}	
R_{OUT1} · R_{OUT2} · R_{OUT3} · R_{OUT4} · R_{OUT5}	Resistance of discharging during cell balance control.
R_{SEL} · R_{CS1} · R_{CS2} · R_{VM1} · R_{VM2}	Resistor to protect terminal.
R_{SDC} · R_{SOC}	Current limitation resistor. (The voltage signal is converted into the current signal by this resistor at the cascading connection.)
C_{COC}	Capacitor to sets discharging overcurrent, charging overcurrent detection/release dead time.
R_{SENSE}	Sense resistance to observe charging/discharging current.
R_{DG1} · R_{DG2}	Resistor for preventing the gate destruction due to parasitic oscillation.
R_{OV1}	Pulldown resistance of OV pin.
R_{REG1}	Resistance of regulator for phase compensation.
R_{REG2}	Resistance of current control when Q4 shorted out.
C_{REG1}	Capacity of regulator for phase compensation.
C_{REG2}	Capacitor to stabilize drain electric potential of Q4.
D1	Diode for preventing backflow from regulator.
D2	Diode for preventing voltage more than VDD pin voltage from applying to OV pin.
Q_1 · Q_2	Nch MOS FET to control discharging current.
Q_3	Nch MOS FET to control charging current.
Q_4	Power transistor of regulator.
Q_5	FET for preventing voltage more than VDD pin voltage from applying to VM1 pin.
Q_6	FET for preventing voltage more than VDD pin voltage from applying to VM2 pin.
Q_{OUT1} · Q_{OUT2} · Q_{OUT3} · Q_{OUT4} · Q_{OUT5}	FET for controling discharging switch during cell balance control.

· 10 cells protection circuit