High voltage 2ch Reset IC with over voltage protection for Automotive

PVT1Cx Series

Overview

This IC is a 40V withstand voltage 2ch voltage detection IC with Over voltage detection that is ideal for monitoring the voltage of car batteries.

The voltage detection accuracy is ± 2% including temperature fluctuation, and the output form is CMOS output. The current consumption is 3.0 μA (typ.), And the operating temperature range is -40 to 105 ° C.

Overview

- Automotive grade (AEC-Q100 Grade2)
- High withstand voltage
- Over voltage detection
- High accuracy detection
- Low current consumption
- Hysteresis voltage selectable (0.1V to 5.0V)

Main specifications

- Maximum rating supply voltage : -0.3V to 40V
- Operating voltage range : 1.8V to 20V
- Operating ambient temperature : -40℃ to 105℃
- Detection voltage : 5.0V to 10.0V (0.1V step)
- Detection voltage accuracy : ±2% (Ta=-40 to 105℃)
- Hysteresis voltage : 0.1V to 5.0V
- OVP detection voltage : 16V to 20V
- OVP detection voltage accuracy : ±4% (Ta=-40 to 105℃)
- Consumption current : Typ. 3.0uA (VDD=3.3V, VS1=VS2=16V)
- Output type : PVT1C1: CMOS
  PVT1C2: Open drain
- Output Logic : PVT1CxA: Ch1 Active L / Ch2 Active L
- Additional function : Separated sense pin

Packages

- SOT-26B

Application

- Voltage monitor for car battery

Model Name

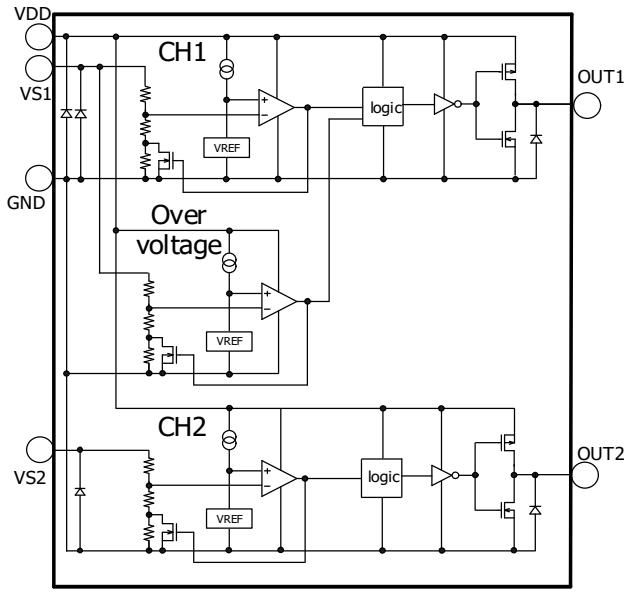
P V T 1 C X X X X N R H

Series name (A) (B) (C) (D) (E) (F) (G)

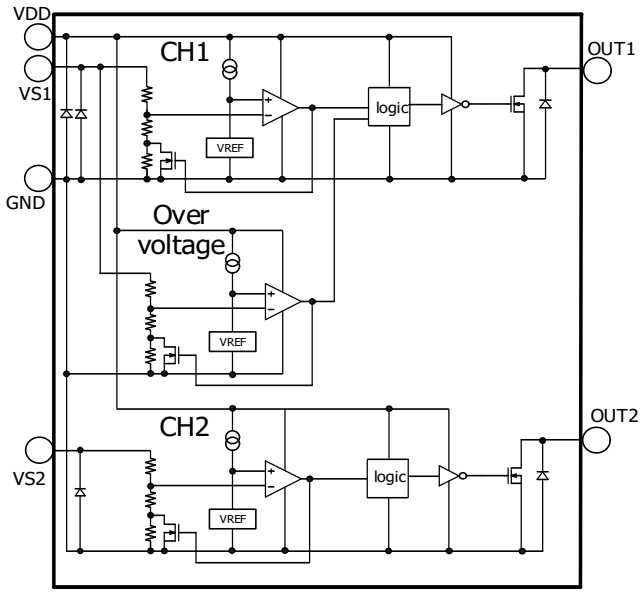
(A)	Function	C	2ch system reset
(B)	Delay function / Output type	1	No delay function / CMOS output
		2	No delay function / Nch open drain output
(C)	Reset output Logic	A	CH1:Low / CH2:Low
		B	CH1:Low / CH2:High
		C	CH1:High / CH2:Low
		D	CH1:High / CH2:High
(D)	Detection voltage and Hysteresis voltage	01	2-digit alphanumerical serial number. ・CH1 and CH2 Reset detect voltage setting range : 5V~10V ・CH1 and CH2 Reset hysteresis voltage setting range : 0.1V~5.0V ・CH1 and CH2 OVP detect voltage setting range : 16V~20V ・CH1 and CH2 OVP hysteresis voltage setting range : 0.5V~1.0V
		≀	
(E)	Package	N	SOT-26B
(F)	Packing specifications 1	R	R housing (Standard)
(G)	Packing specifications 2	H	Embos tape / Halogen free

Block Diagram

■ PST1C1 (CMOS output)

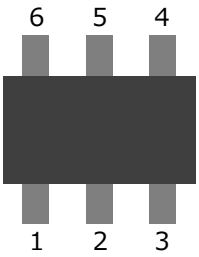


■ PST1C2 (Nch open drain output)



Pin Configuration

- SOT-26B



Top view

Pin No.	Pin name	Function
1	VS2	CH2 Voltage sensing pin
2	OUT2	CH2 Output pin
3	VS1	CH1 Voltage sensing pin
4	VDD	Power supply input pin
5	GND	Ground pin
6	OUT1	CH1 Output pin

Absolute Maximum Ratings

Item		Symbol	Min.	Max.	Unit
Supply voltage		VDD	-0.3	40	V
VS1 pin voltage		VS1	-0.3	40	V
VS2 pin voltage		VS2	-0.3	40	V
OUT1 pin voltage	PVT1C1	VOUT1	-0.3	VDD+0.3	V
	PVT1C2	VOUT1	-0.3	40	V
OUT2 pin voltage	PVT1C1	VOUT2	-0.3	VDD+0.3	V
	PVT1C2	VOUT2	-0.3	40	V
OUT1 pin output current		IOUT1	-	20	mA
OUT2 pin output current		IOUT2	-	20	mA
Storage temperature		Tstg	-55	150	℃
Power dissipation		Pd1	-	150	mW

Recommended Operating Conditions

Item	Symbol	Min.	Max.	Unit
Operating ambient temperature	Topr	-40	105	℃
Operating voltage	Vop	2.7	20	V

Electrical Characteristics

(Ta=-40~105°C, typically value at VDD=3.3V, Ta=25°C, unless otherwise specified)

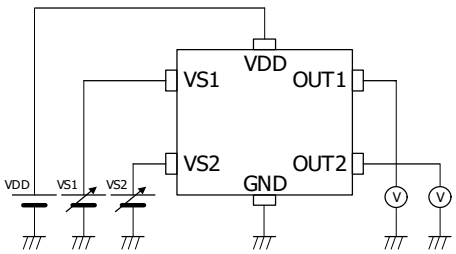
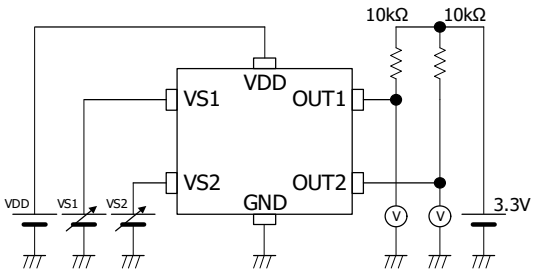
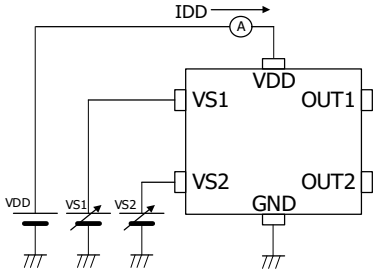
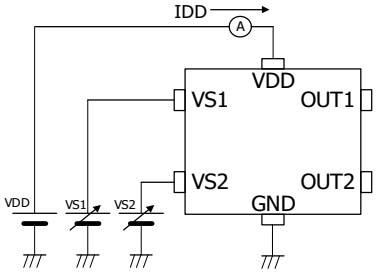
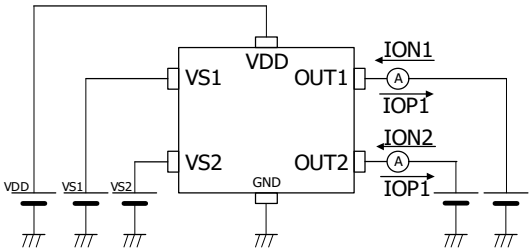
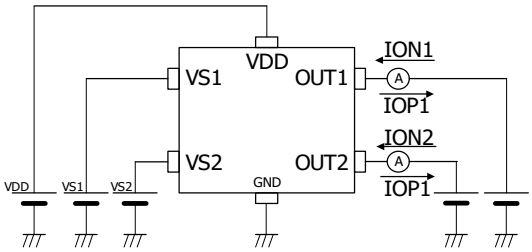
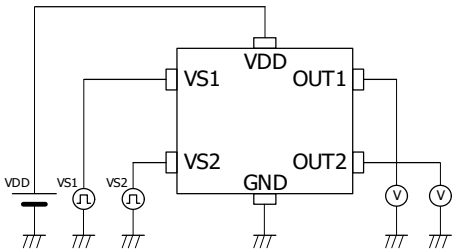
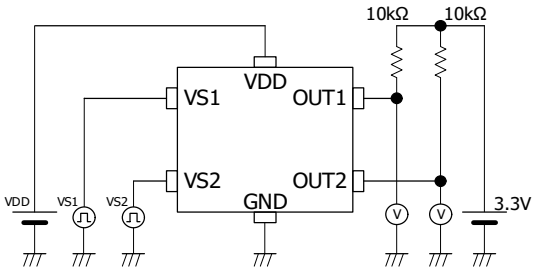
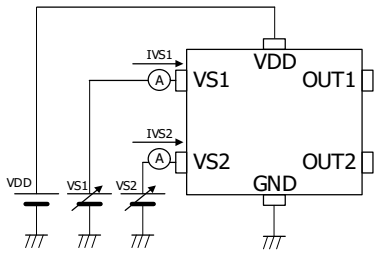
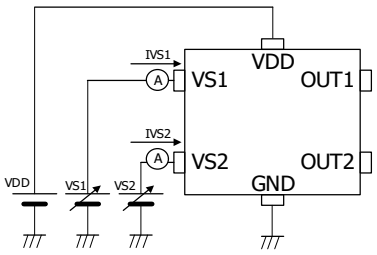
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
CH1 Reset voltage	VTH1	VDD=3.3V, VS1:H→L		VTH1×0.98	VTH1	VTH1×1.02	V	A
CH1 Hysteresis voltage	ΔVTH1	VDD=3.3V ΔVTH1=VRE1-VTH1		-	ΔVTH1	-	V	A
CH1 Release voltage	VRE1	VDD=3.3V, VS1:L→H	ΔVTH1 <1.0V	VTH1×0.98 + ΔVTH1-0.1	VTH1 + ΔVTH1	VTH1×1.02 + ΔVTH1+0.1	V	A
			ΔVTH1 ≧1.0V	VTH1×0.98 + ΔVTH1×0.9	VTH1 + ΔVTH1	VTH1×1.02 + ΔVTH1×1.1	V	A
CH1 OVP detect voltage	Vovr	VDD=3.3V, VS1=L→H		Vovr×0.96	Vovr	Vovr×1.04	V	A
CH1 OVP Hysteresis voltage	ΔVov	VDD=3.3V ΔVov=Vovr-Vovf		-	ΔVov	-	V	A
CH1 OVP release voltage	Vovf	VDD=3.3V, VS1=H→L		Vovr×0.96 + ΔVov-0.1	Vovr + Δvov	Vovr×1.04 + Δvov+0.1	V	A
CH2 Reset voltage	VTH2	VDD=3.3V, VS2:H→L		VTH2×0.98	VTH2	VTH2×1.02	V	A
CH2 Hysteresis voltage	ΔVTH2	VDD=3.3V ΔVTH2=VRE2-VTH2		-	ΔVTH2	-	V	A
CH2 Release voltage	VRE2	VDD=3.3V, VS2:L→H	ΔVTH2 <1.0V	VTH2×0.98 + ΔVTH2-0.1	VTH2 + ΔVTH2	VTH2×1.02 + ΔVTH2+0.1	V	A
			ΔVTH2 ≧1.0V	VTH2×0.98 + ΔVTH2×0.9	VTH2 + ΔVTH2	VTH2×1.02 + ΔVTH2×1.1	V	A

Electrical Characteristics

(Ta=-40~105°C, typically value at VDD=3.3V, Ta=25°C, unless otherwise specified)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Consumption current	IDD	VDD=3.3V, VS1=16V, VS2=16V		-	3	6	μA	B
CH1 Nch Output current	ION1	VDD=3.3V VS1=0V, VOUT1=0.5V	PVT1CxA PST1CxB	0.1	1	-	mA	C
		VDD=3.3V VS1=16V, VOUT1=0.5V	PVT1CxC PST1CxD	0.1	1	-	mA	C
CH2 Nch Output current	ION2	VDD=3.3V VS2=0V, VOUT2=0.5V	PVT1CxA PST1CxC	0.1	1	-	mA	C
		VDD=3.3V VS2=16V, VOUT2=0.5V	PVT1CxB PST1CxD	0.1	1	-	mA	C
CH1 Pch Output current	IOP1	VDD=3.3V VS1=16V, VOUT2=2.8V	PVT1C1A PST1C1B	0.1	0.4	-	mA	C
		VDD=3.3V VS1=0V, VOUT2=2.8V	PVT1C1C PST1C1D	0.1	0.4	-	mA	C
CH2 Pch Output current	IOP2	VDD=3.3V VS2=16V, VOUT2=2.8V	PVT1C1A PST1C1C	0.1	0.4	-	mA	C
		VDD=3.3V VS2=0V, VOUT2=2.8V	PVT1C1B PST1C1D	0.1	0.4	-	mA	C
CH1 Output leakage current	ILEAK1	VDD=20V VS1=20V, VOUT1=20V	PVT1C2A PST1C2B	-	-	2	uA	C
		VDD=20V VS1=0V, VOUT1=20V	PVT1C2C PST1C2D	-	-	2	uA	C
CH2 Output leakage current	ILEAK2	VDD=20V VS2=20V, VOUT2=20V	PVT1C2A PST1C2C	-	-	2	uA	C
		VDD=20V VS2=0V, VOUT2=20V	PVT1C2B PST1C2D	-	-	2	uA	C
CH1 Reset transfer delay time	TdHLC1	VDD=3.3V VS1=13V→0V		1	-	200	μs	D
CH2 Reset transfer delay time	TdHLC2	VDD=3.3V VS2=13V→0V		1	-	200	μs	D
CH1 Release transfer delay time	TdLHC1	VDD=3.3V VS1=0V→13V		1	-	150	μs	D
CH2 Release transfer delay time	TdLHC2	VDD=3.3V VS2=0V→13V		1	-	150	μs	D
VS1 pin resistance	RVS1	VDD=3.3V VS1=14V		5	-	100	MΩ	E
VS2 pin resistance	RVS2	VDD=3.3V VS2=14V		10	-	100	MΩ	E

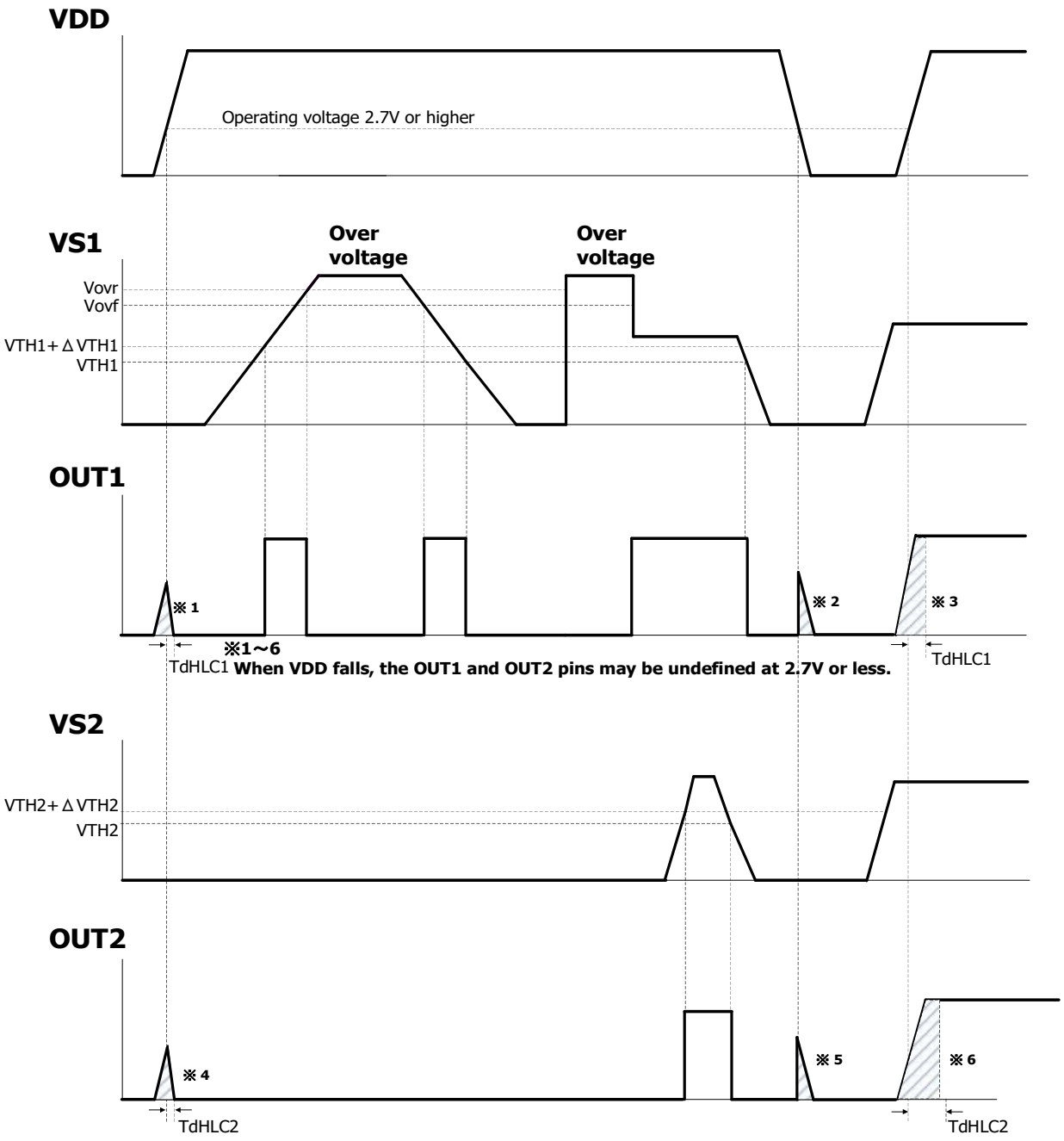
Test Circuit

	PST1C1 (CMOS output)	PST1C2 (Nch Open drain output)
A		
B		
C		
D		
E		

Timing Chart

- PST1C1A

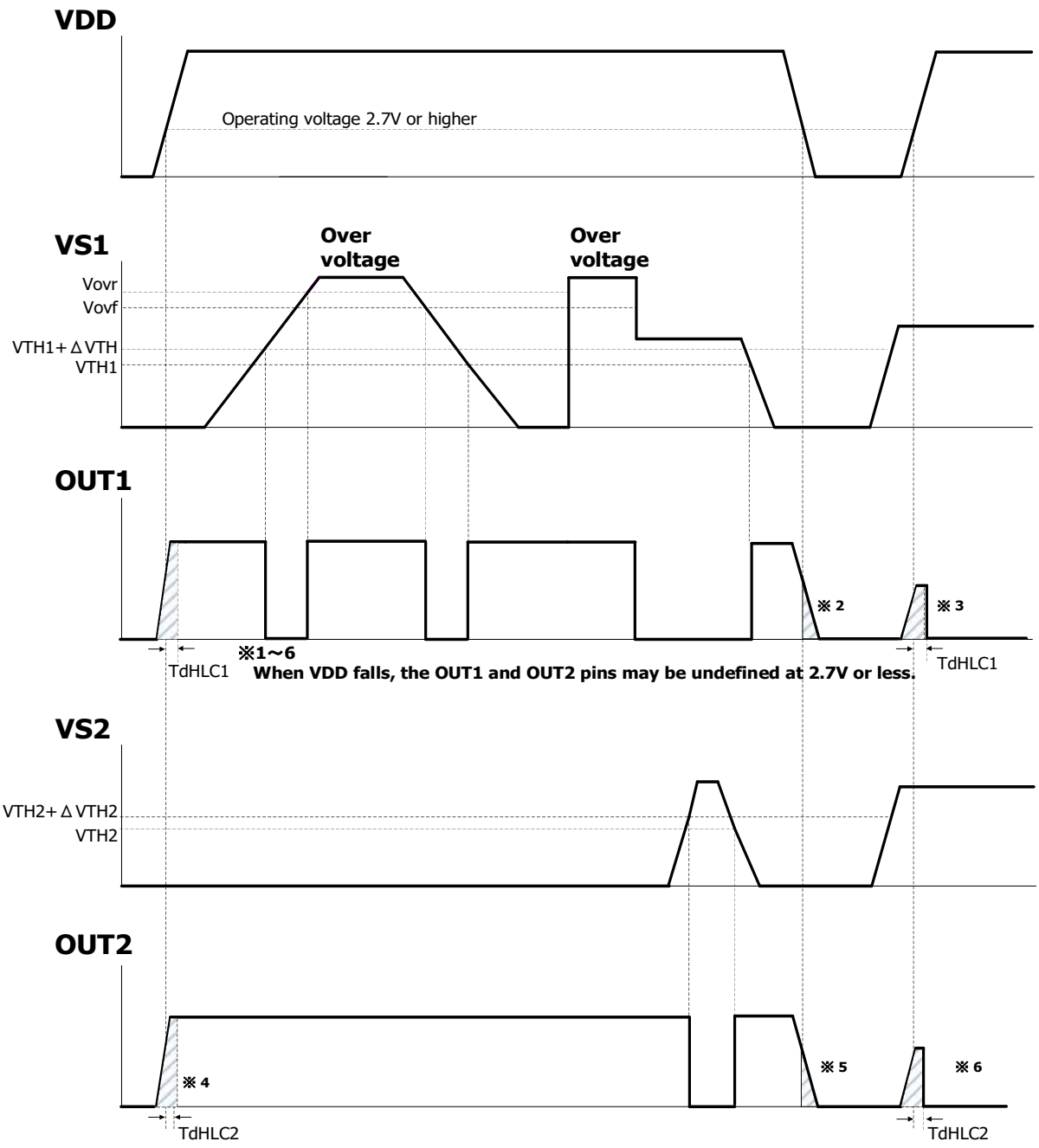
ch1 OUT1=Low at reset or OVP detect / OUT2=Low at reset detect



Timing Chart

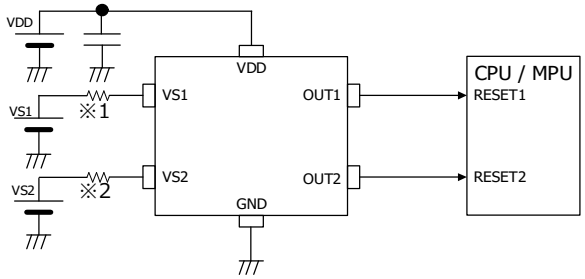
- PST1C2D

ch1 OUT1=High at reset or OVP detect / OUT2=High at reset detect

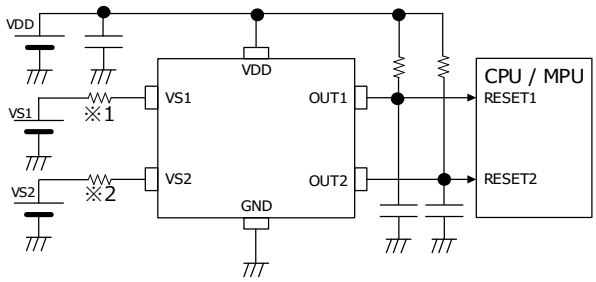


Application Circuit

- PST1C1 (CMOS output)



- PST1C2 (Nch open drain output)



※1、2 Current limiting resistor for negative surge protection.

Note

1. The typical application circuit is not guaranteed for a set applications. It has to test sufficiently in a set applications.

2. In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi shall not be liable for any such problem, nor grant a license therefore.

3. For Surge and over voltage protection, recommend to use ESD protection device such as baristor at battery pin (ex. VS1, VS2).
   At the negative surge, the reset output may be erroneously output,
   so please consider countermeasures using external components
   depending on the required specifications of the set circuit.

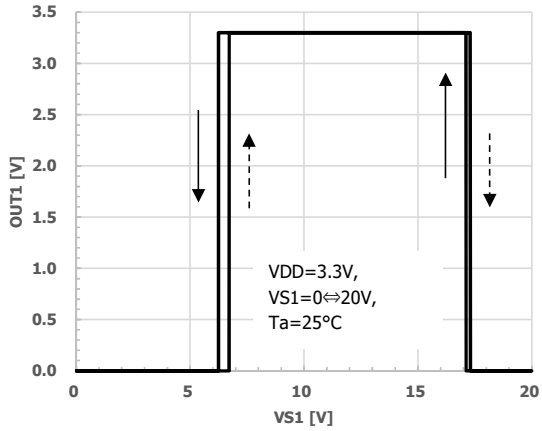
4. At VDD start-up, the output may be undifiend during the transfer delay. After VDD exceeds 2.7V, It is recommended to set the output to wait during reset and release transfer delay time.
   When VDD falls, the OUT1 and OUT2 pins may be undefined at 2.7V or less.

5. Between next to each other pin of PVT1xx (SOT-26B), it has parasitic capacitance due to Package and IC round, max 0.2pF . Because of next to VS pin and OUT pin, when it happened VS pin voltage is changing rapidly, it afferd between pin, it happened over / under shoot.
   When it may have parasitic capacitance to OUT pin round at set board, it improves layout pattern, separating from changing rapidly node or adding shield of ground.

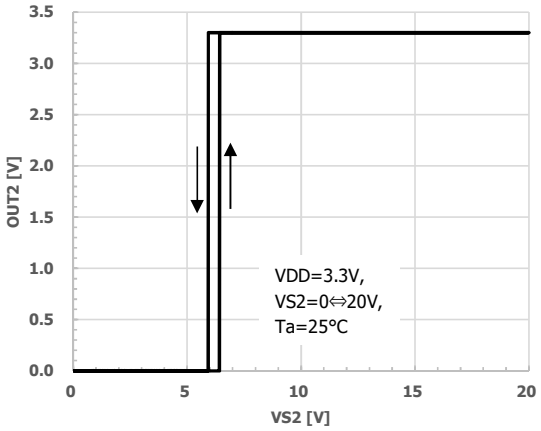
Typical Performance Characteristics

PVT1C1A01N : VTH1=6.2V, ΔVTH1=0.5V, VTH2=5.9V, ΔVTH2=0.6V

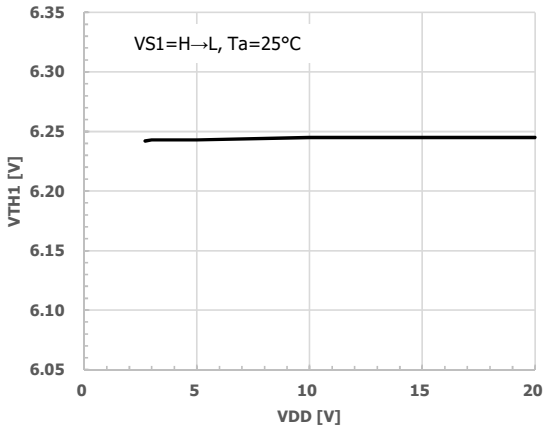
■ CH1 reset voltage - VS1



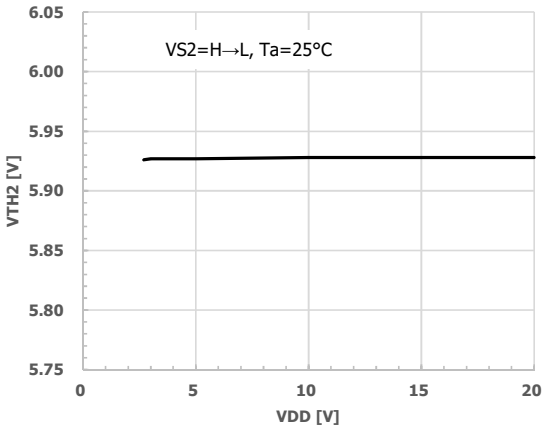
■ CH2 reset voltage - VS2



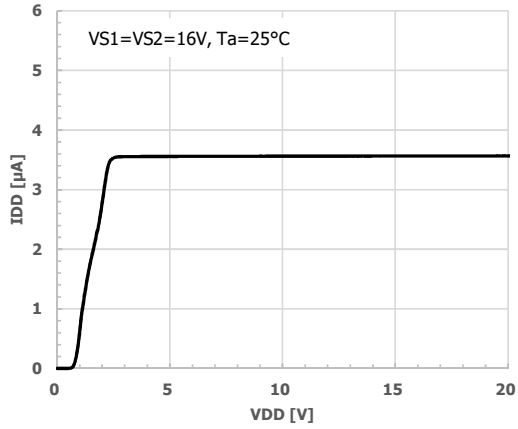
■ CH1 reset voltage -VDD



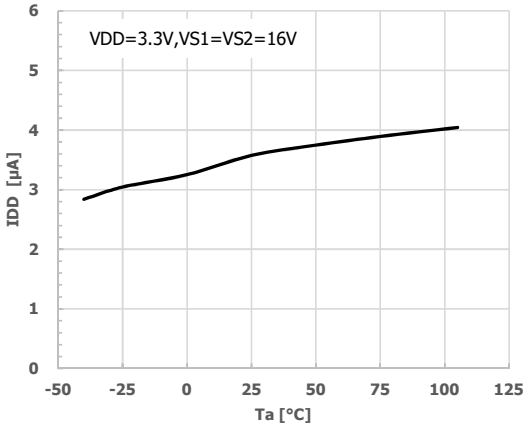
■ CH2 reset voltage -VDD



■ Supply current - VDD



■ Supply current - Temperature

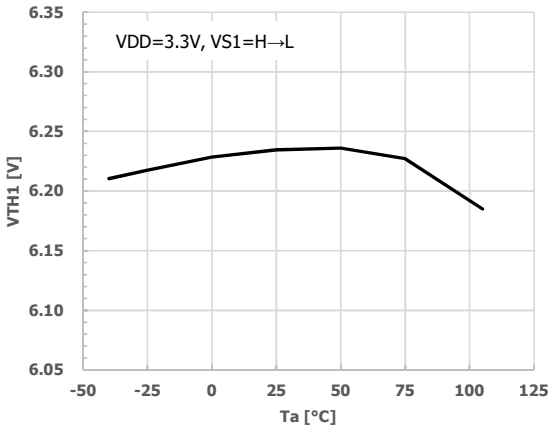


*The above characteristics are typical values.

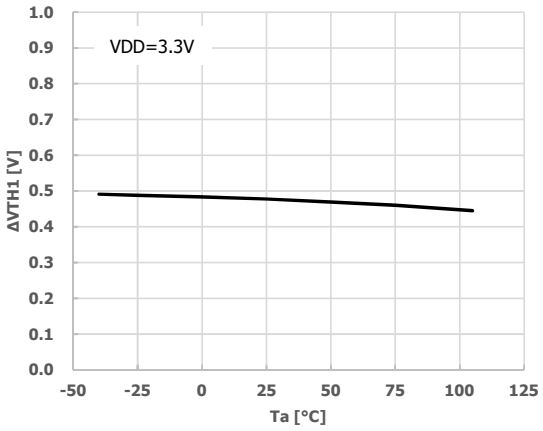
Typical Performance Characteristics

PVT1C1A01N : VTH1=6.2V, ΔVTH1=0.5V, VTH2=5.9V, ΔVTH2=0.6V

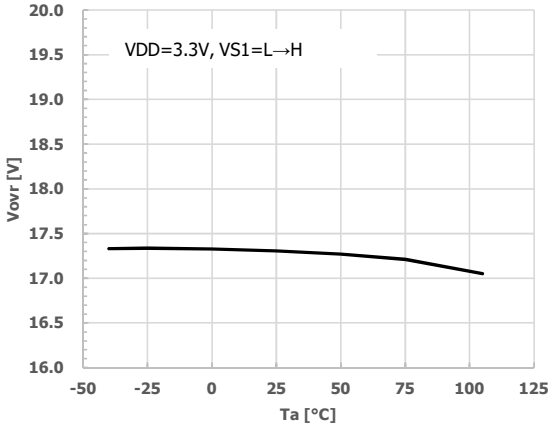
■ CH1 reset voltage - Temperature



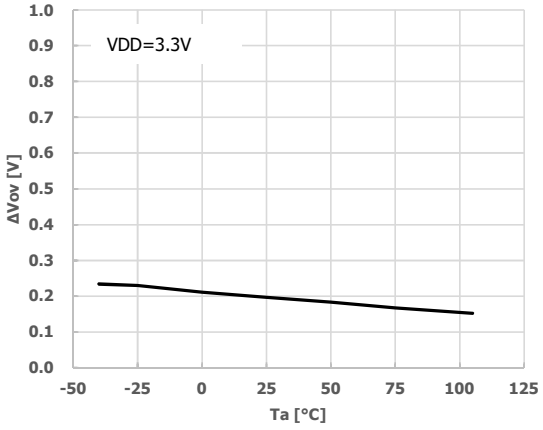
■ CH1 hysteresis voltage - Temperature



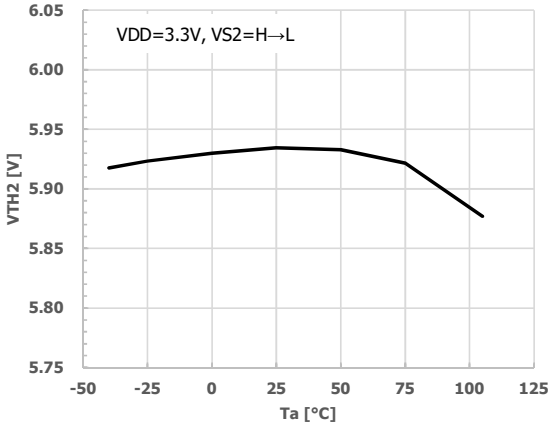
■ CH1 over voltage rising - Temperature



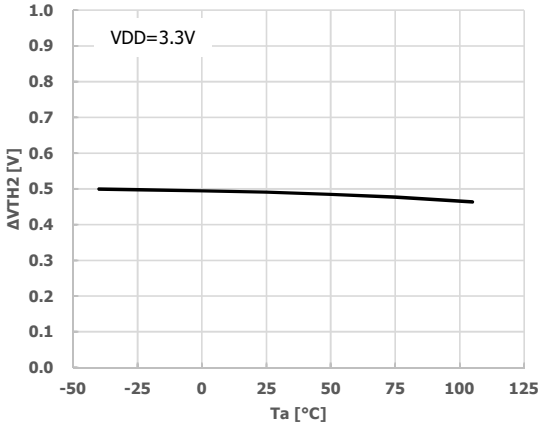
■ CH1 over voltage hysteresis voltage - Temperature



■ CH2 reset voltage - Temperature



■ CH2 hysteresis voltage - Temperature

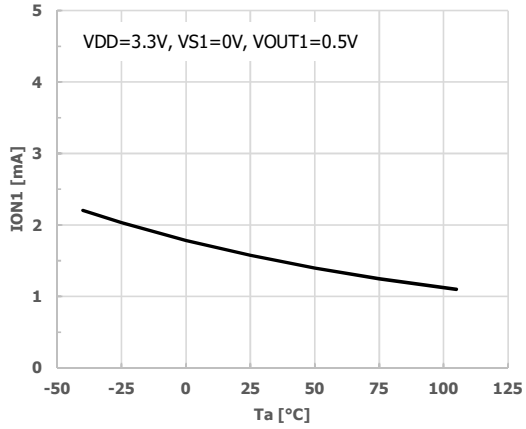


*The above characteristics are typical values.

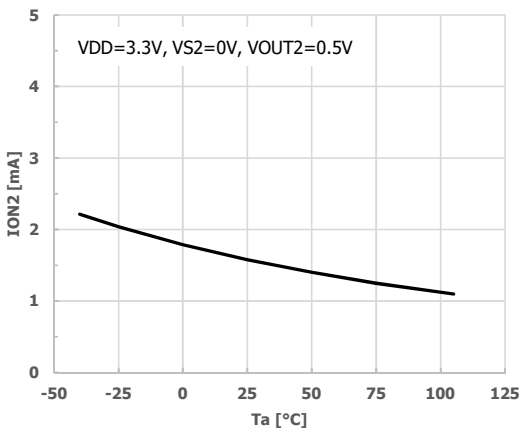
Typical Performance Characteristics

PVT1C1A01N : VTH1=6.2V, ΔVTH1=0.5V, VTH2=5.9V, ΔVTH2=0.6V

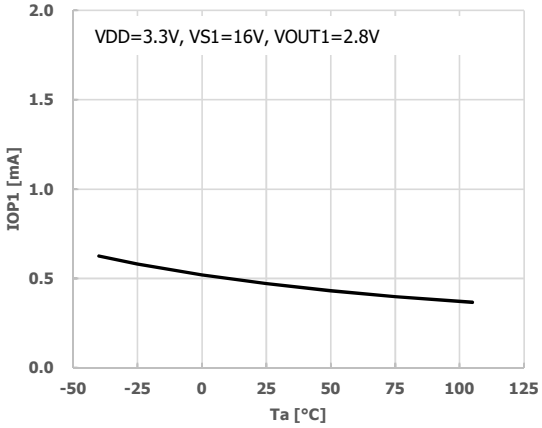
■ CH1 Nch output current - Temperature



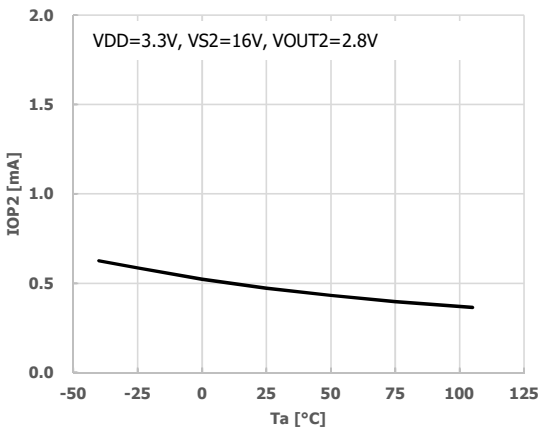
■ CH2 Nch output current - Temperature



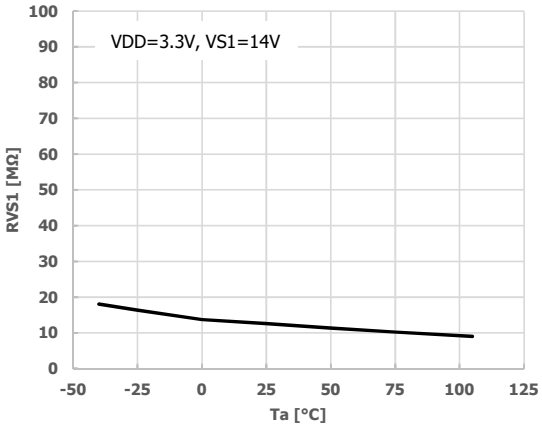
■ CH1 Pch output current - Temperature



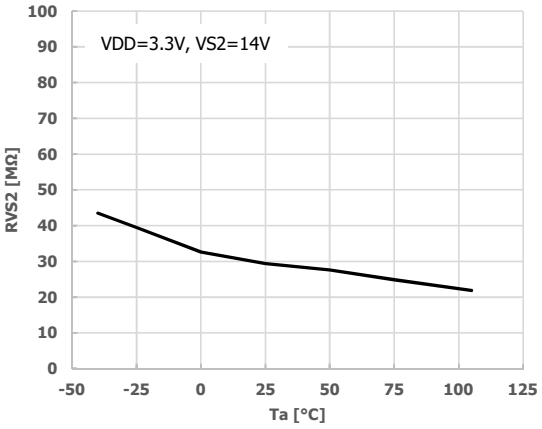
■ CH2 Pch output current - Temperature



■ VS1 pin resistance - Temperature



■ VS2 pin resistance - Temperature

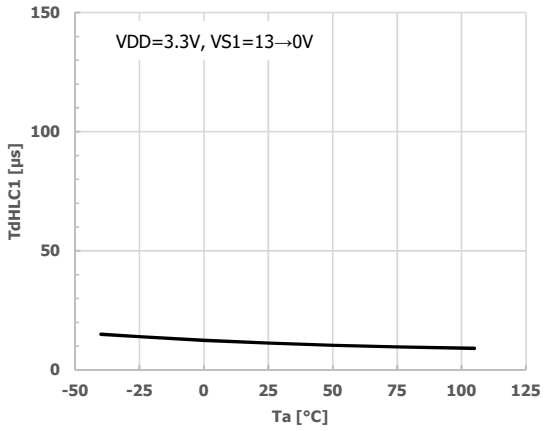


*The above characteristics are typical values.

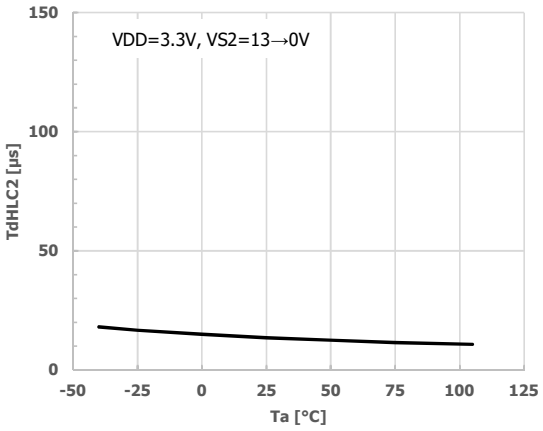
Typical Performance Characteristics

PVT1C1A01N : VTH1=6.2V, ΔVTH1=0.5V, VTH2=5.9V, ΔVTH2=0.6V

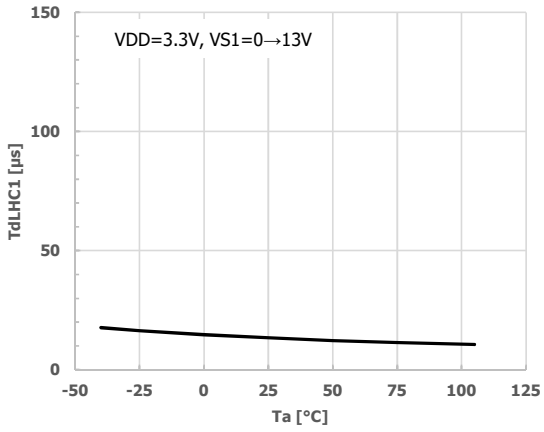
■ CH1 reset transfer delay time - Temperature



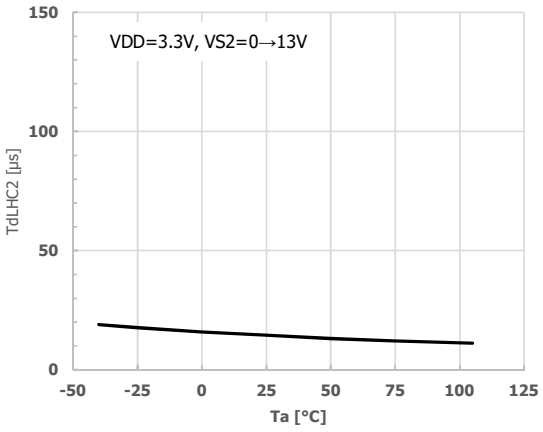
■ CH2 reset transfer delay time - Temperature



■ CH1 release transfer delay time - Temperature



■ CH2 release transfer delay time - Temperature



*The above characteristics are typical values.