MITSUMI

Supercapacitor charge/discharge control IC for power supply backup

MM4039XR

Description

This is a control IC that manages the charging and discharging of power backup supercapacitors in both 3.3V and 5V systems. Its function is to charge the supercapacitor while simultaneously supplying power from the input power supply to the system. In the event of a power supply failure, it seamlessly switches to backup operation, supplying power from the supercapacitor to the system. During a power outage, the IC will switch to backup operation and use power from the super capacitor to sustain the system. This allows for a safe shutdown of the microcontroller, memory, and other components.

Applications

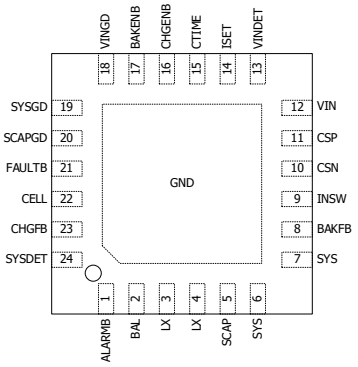
Surveillance cameras, Industrial IoT equipment,
Handy Terminal for business use, Capacitor UPS, etc.

Features

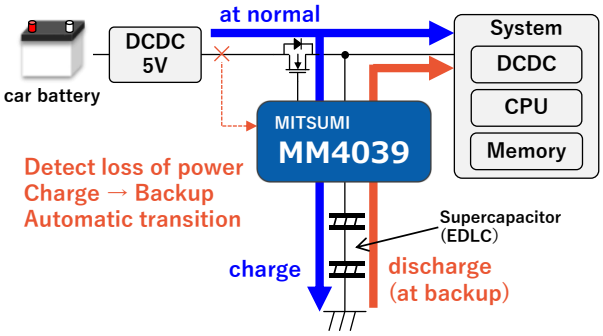
1. Easily enables power supply backup applications using supercapacitors
2. Built-in charge pump to drive the input load switch
3. Input current distribution function that prioritizes system power supply (IINDPM function)
4. 13V input rating with input over voltage protection
5. Input overcurrent protection
6. Small package（4.0mm x 4.0mm x 0.75mm)
7. Operating ambient temperature Ta=-40～105℃

Package

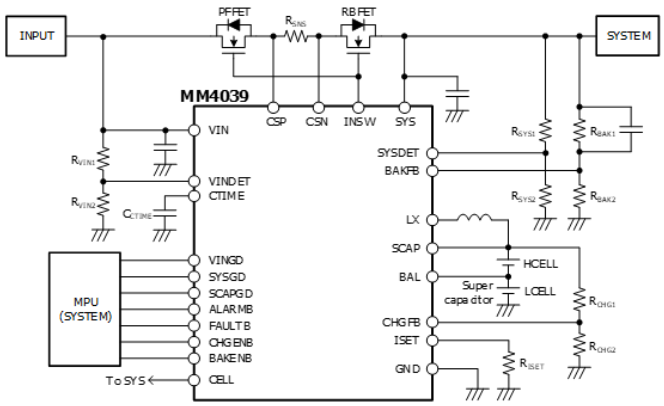
SQFN-24A (4.0mm x 4.0mm x 0.75mm)



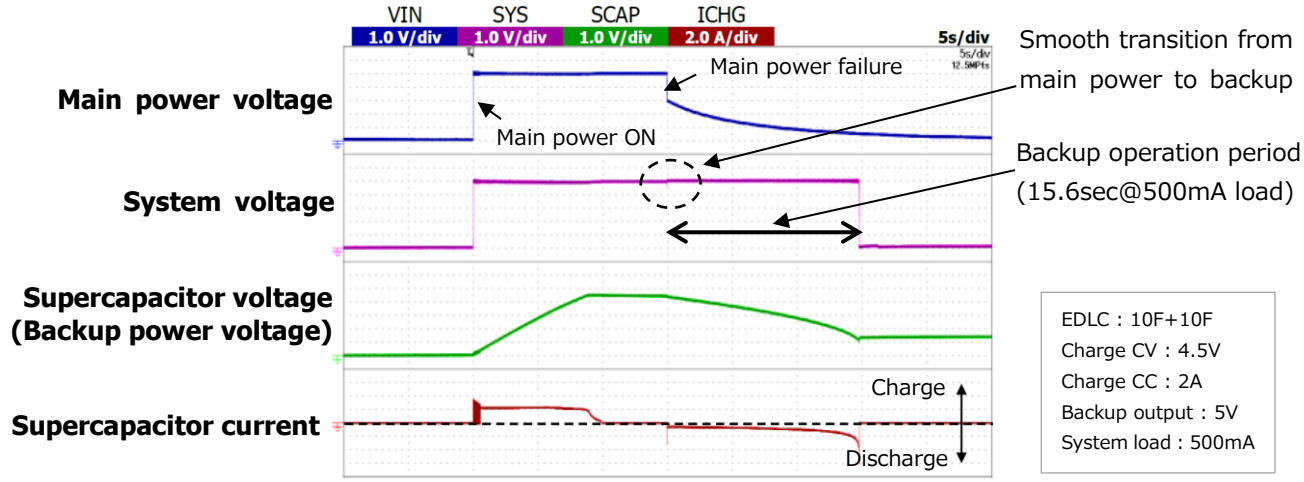
Example of use (Drive Recorder)



Application circuit example



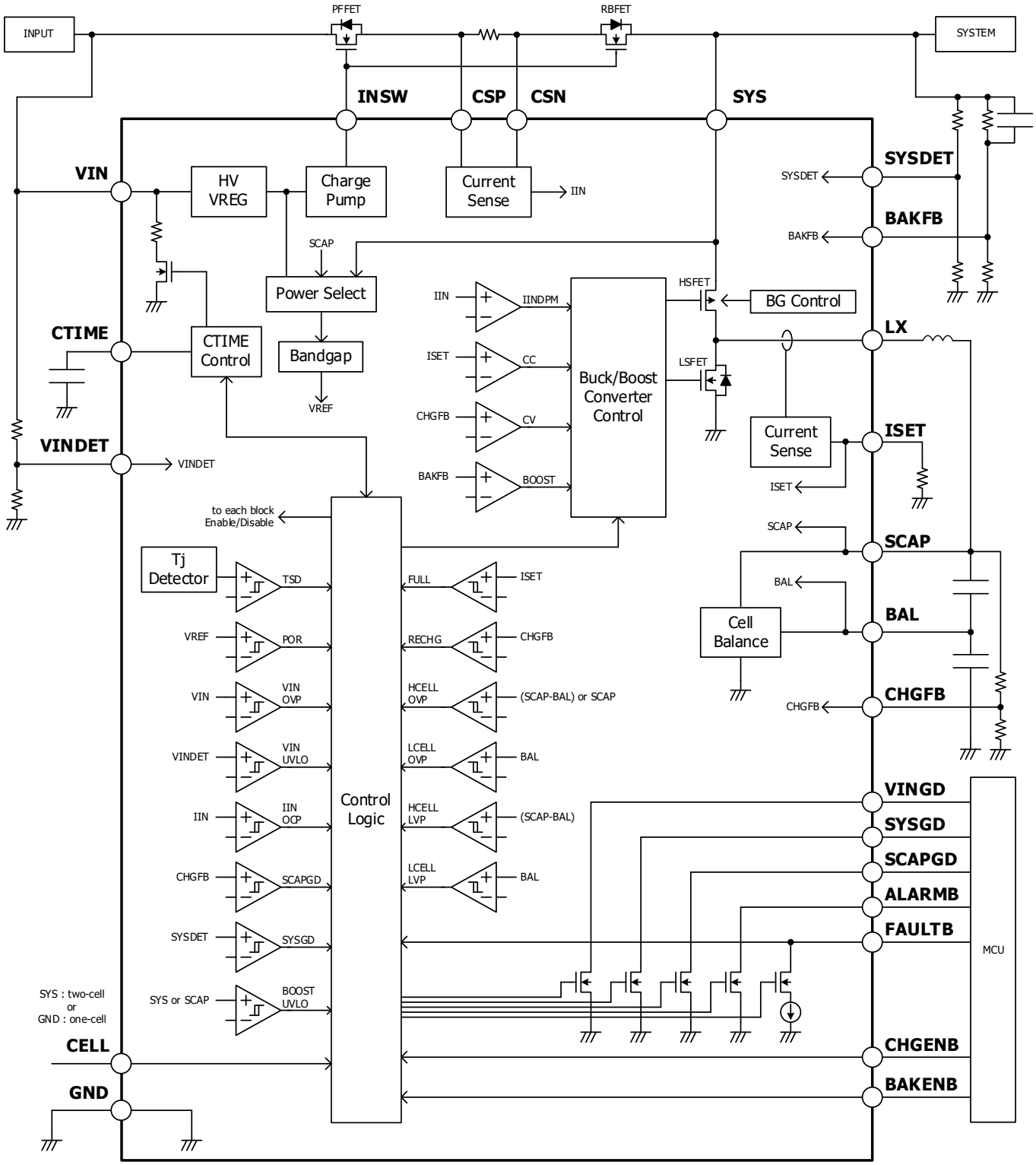
Typical Characteristics



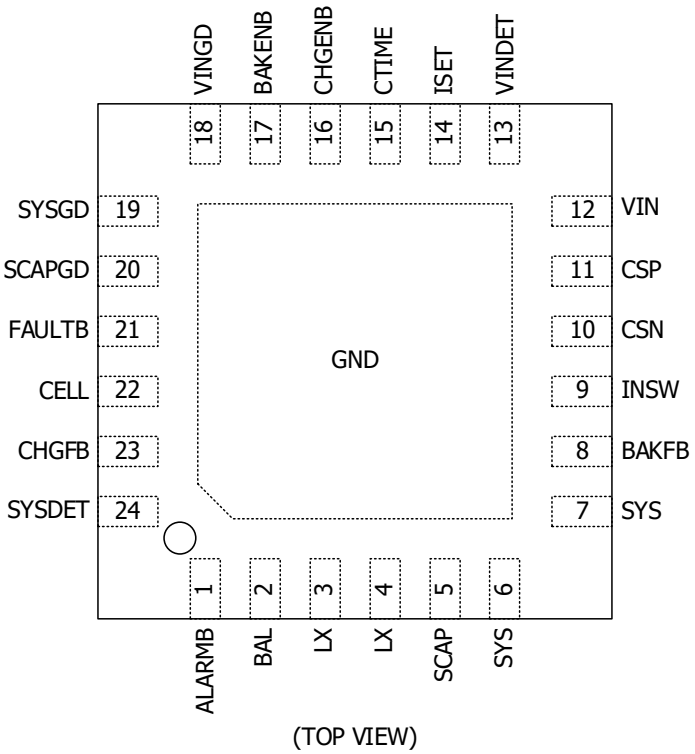
EDLC : 10F+10F
Charge CV : 4.5V
Charge CC : 2A
Backup output : 5V
System load : 500mA

MITSUMI ELECTRIC CO., LTD.
Semiconductor Business Unit
Strategy Engineering Department
tel:+81-46-230-3470

1. BLOCK DIAGRAM



2. PIN CONFIGURATION



(TOP VIEW)

3. PIN DESCRIPTION

Pin No.	Pin Name	Pin Description
1	ALARMB	System protection function indicator. It is NMOS open drain output. "Hi-Z" in normal operation, "Low" in protection operation. For details, see 8-7-2 on page 15.
2	BAL	Cell balance pin. When CELL = "H" (two-cell selection), the midpoints of the two supercapacitors is connected. When CELL = "L" (one-cell selection), it is open or connected to GND.
3,4	LX	DC-DC converter inductor connection pin.
5	SCAP	Supercapacitor connection pin. Connects the positive side of the supercapacitor.
6,7	SYS	System connection pin. In charging mode, this pin is the power input pin for charging. In backup mode, this pin serves as the power output pin for the system.
8	BAKFB	Feedback pin for backup boost DC-DC converter. Connect resistor R_{BAK1} to SYS and resistor R_{BAK2} to GND. For details, see 8-4 on page 14.
9	INSW	Charge pump output pin for driving input load switch. Connects to the gate of an external NchFET.
10	CSN	Input current sense negative pin. Connect sense resistor R_{SNS} to CSP. For details, see 8-3-1 on page 13 and 8-7-2 on page 15.
11	CSP	Input current sense positive pin. Connect sense resistor R_{SNS} to CSN. For details, see 8-3-1 on page 13 and 8-7-2 on page 15.
12	VIN	Input power supply connection pin.
13	VINDET	Input power supply detection pin. Connect resistor R_{VIN1} to VIN and resistor R_{VIN2} to GND. For details, see 8-2 on page 13 and 8-6-1 on page 15.
14	ISET	Charging current setting pin. Connect resistor R_{ISET} to GND. For details, see 8-3-1 on page 13.

Pin No.	Pin Name	Pin Description
15	CTIME	Mode switching dead time setting pin. Connect capacitance C_{CTIME} to GND. For details, see 8-4 on page 14.
16	CHGENB	Active-low charge operation enable pin. "H/L" input.
17	BAKENB	Active-low backup operation enable pin. "H/L" input.
18	VINGD	VINDET voltage indicator. NMOS open drain output. For details, see 8-6-1 on page 15.
19	SYSGD	SYSDET voltage indicator. NMOS open drain output. For details, see 8-6-2 on page 15.
20	SCAPGD	CHGFB voltage indicator. NMOS open drain output. For details, see 8-6-3 on page 15.
21	FAULTB	Supercapacitor protection indicator. For details, see 8-7-1 on page 15.
22	CELL	Supercapacitor one-cell / two-cell selection pin." H/L" input. For details, see 8-1 on page 13.
23	CHGFB	Feedback pins for charge buck DC-DC converter. Connect resistor R_{CHG1} to SCAP and resistor R_{CHG2} to GND. For details, see 8-3-1 on page 13.
24	SYSDET	System voltage detection pin. Connect resistor R_{SYS1} to SYS and resistor R_{SYS2} to GND. For detail, see 8-6-2 on page 15.
Exposed pad	GND	Ground pin. It also serves as a heat radiation PAD. It is recommended to connect to the board ground plane.

4. ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified : Ta = 25°C)

Parameter		Symbol	Min.	Max.	Units
Storage temperature		Tstg	-55	150	°C
Junction temperature		Tj_{MAX}	-40	150	°C
Input voltage	ALARMB, VIN	Vin_{MAX1}	-0.3	13	V
	Other than above	Vin_{MAX2}	-0.3	6	V
Sink current	ALARMB, VINGD, SYSGD, SCAPGD	$Isink_{MAX}$	-	15	mA
Power dissipation	Board mounted(*1)	Pd	-	2.5	W

(*1) Board size : 70 mm × 70 mm × 0.8 mm Material : glass epoxy Layer : 4 Layers Copper foil area : 90%

5. RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified : Ta = 25°C)

Parameter		Symbol	Min.	Max.	Units
Operating ambient temperature(*2)		Topr	-40	105	°C
Junction temperature		Tj	-40	125	°C
Input voltage	VIN	V_{VIN}	3	5.6	V
Output current	Buck converter (Charging current)	I_{OUT1}	-	2.5	A
	Boost converter (Backup current)	I_{OUT2}	-	2.5	A
ISET resistor		R_{ISET}	0.96	4.8	kΩ

(*2) Board size : 70 mm × 70 mm × 0.8 mm Material : glass epoxy Layer : 4 Layers Copper foil area : 90%

6. ELECTRICAL CHARACTERISTICS

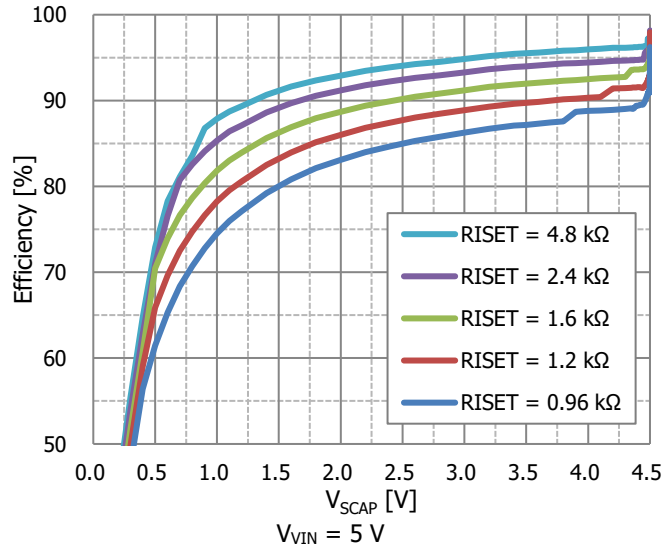
(Unless otherwise specified : V_{VIN} = 5 V, V_{SCAP} = 2.5 V, Ta = 25°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
CURRENT CONSUMPTION						
Power-on reset	V_{POR}	(The higher voltage of V_{VIN} and V_{SYS} and V_{SCAP}) rising	2.5	2.6	2.7	V
Current consumption in charging mode	I_{VIN1}	VIN pin, V_{VIN} = 5 V, CELL = "H", charging terminated	-	120	200	μA
	I_{SYS1}	SYS pin, V_{VIN} = 5 V, V_{SYS} = 5 V, CELL = "H", charging terminated, BAKENB = "L"	-	95	160	μA
	I_{SYS2}	SYS pin, V_{VIN} = 5 V, V_{SYS} = 5 V, CELL = "H", charging terminated, BAKENB = "H"	-	5	10	μA
	I_{SCAP1}	SCAP pin, V_{VIN} = 5 V, V_{SCAP} = 4.5 V, CELL = "H", charging terminated	-	2.5	5	μA
Current consumption in backup mode	I_{SYS3}	SYS pin, V_{VIN} = 0 V, V_{SCAP} = 4.5 V, CELL = "H", converter not switching	-	65	110	μA
	I_{SCAP2}	SCAP pin, V_{VIN} = 0 V, V_{SCAP} = 4.5 V, CELL = "H", converter not switching	-	1	2	μA
Current consumption in shutdown mode	I_{VIN2}	VIN pin, V_{VIN} = 5 V, V_{SCAP} = 4.5 V, CHGENB = BAKENB = CELL = "H"	-	40	60	μA
	I_{SCAP3}	SCAP pin, V_{VIN} = 5 V, V_{SCAP} = 4.5 V, CHGENB = BAKENB = CELL = "H"	-	3.5	7	μA
Discharge current in shutdown mode	I_{CS}	CSP pin + CSN pin, V_{CSP} = V_{CSN} = 5 V, CHGENB = BAKENB = CELL = "H"	-	10	20	mA
CHARGING MODE (BUCK SWITCHING)						
Input current limit regulation voltage	V_{IINDPM}	V_{CSP} - V_{CSN}	18.8	20	21.2	mV
CHGFB servo voltage	$V_{FB(CHG)}$		788.5	800	811.5	mV
CHGFB input leakage current	$I_{FB(CHG)}$		-40	-	40	nA
SCAP regulation voltage setting range	V_{REG_RNG}		2	-	4.5	V
Charge current setting range	I_{CHG_RNG}		0.5	-	2.5	A
Charge current formula	I_{CHG}	V_{SCAP} = 2.8 V	2400 / R_{ISET}			A
Charge current accuracy 1 (% of setting)	I_{CHG_ACC1}	V_{SCAP} = 2.8 V, R_{ISET} < 2 kΩ	-5	-	+5	%
	I_{CHG_ACC2}	V_{SCAP} = 2.8 V, R_{ISET} ≥ 2 kΩ	-7.5	-	+7.5	%
Charge current accuracy 2 (offset)	I_{CHG_OFFSET}	V_{SCAP} = 2.8 V ex) when R_{ISET} < 2 kΩ Min. : -5% -40 mA Max. : +5% +40 mA	-40	-	40	mA
ISET servo voltage	$V_{ISET(CHG)}$	V_{ISET} when charging with I_{CHG}	-	800	-	mV
Full charge detection voltage	V_{EOC}	When detect V_{ISET} < V_{EOC} , full charge is determined.	-	100	-	mV
Full charge detection deglitch time	t_{EOC}		-	5	-	ms
Recharge detection voltage	V_{RECHG}	V_{CHGFB} falling, As Percentage to $V_{FB(CHG)}$	96.25	97.5	98.75	%
Recharge detection deglitch time	t_{RECHG}		-	5	-	ms
BAL servo voltage	V_{BALV}		-50	V_{SCAP} × 0.5	+50	mV
セルバランス ソース電流 BAL source current	$I_{BALSOURCE}$	V_{SCAP} = 4.5 V, V_{BAL} = V_{BALV} - 0.1 V	-	50	-	mA
BAL sink current	$I_{BALSINK}$	V_{SCAP} = 4.5 V, V_{BAL} = V_{BALV} + 0.1 V	-	50	-	mA
SYS-SCAP differential UVLO	$V_{UVLO(CHG)}$	(V_{SYS} - V_{SCAP}) falling	10	50	90	mV
Hysteresis on $V_{UVLO(CHG)}$	$V_{UVLO(CHG)\_HYS}$	(V_{SYS} - V_{SCAP}) rising	100	150	200	mV
Switching frequency in charging mode	$f_{LX(CHG)}$		2	2.25	2.5	MHz
ON resistance of HSFET in charging mode	$R_{HS(CHG)}$		-	135	-	mΩ
ON resistance of LSFET in charging mode	$R_{LS(CHG)}$		-	55	-	mΩ
Charge overcurrent detection	$I_{OCP(CHG)}$		3	4.5	-	A

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Charge overvoltage detection	$V_{SCAPOVP}$	(V_{SCAP} - V_{BAL}) rising or V_{BAL} rising, CELL = "H" V_{SCAP} rising, CELL = "L"	2.6	2.7	2.8	V
Hysteresis on $V_{SCAPOVP}$	$V_{SCAPOVP\_HYS}$		-	60	-	mV
BACKUP MODE (BOOST SWITCHING)						
BAKFB servo voltage	$V_{FB(BAK)}$		781	800	819	mV
BAKFB input leakage current	$I_{FB(BAK)}$		-40	-	40	nA
Backup output voltage setting range	V_{BAK_RNG}		2.7	-	5	V
UVLO in backup mode	$V_{UVLO(BAK)}$	(The higher voltage of V_{SYS} and V_{SCAP}) falling	2.35	2.45	2.55	V
Hysteresis on $V_{UVLO(BAK)}$	$V_{UVLO(BAK)\_HYS}$		-	0.15	-	V
Switching frequency in backup mode	$f_{LX(BAK)}$		1	1.125	1.25	MHz
ON resistance of HSFET in backup mode	$R_{HS(BAK)}$		-	55	-	mΩ
ON resistance of LSFET in backup mode	$R_{LS(BAK)}$		-	55	-	mΩ
Backup overcurrent detection	$I_{OCP(BAK)}$		5.5	6.5	7.5	A
Backup overvoltage detection	V_{SYSOVP}	V_{SYS} rising	5.3	5.5	5.7	V
Hysteresis on V_{SYSOVP}	V_{SYSOVP_HYS}		-	0.1	-	V
Backup input low-voltage detection	$V_{SCAPLVP}$	(V_{SCAP} - V_{BAL}) falling or V_{BAL} falling, CELL = "H"	0	60	-	mV
Hysteresis on $V_{SCAPLVP}$	$V_{SCAPLVP\_HYS}$		-	50	-	mV
Mode switching dead time	t_{CTIME}	C_{CTIME} = 1 nF	-	1.9	-	ms
VIN pulldown resistance	$R_{VINPULL}$	V_{VIN} = 5 V in mode switching dead time	-	150	-	Ω
VOLTAGE DETECTION COMPARATOR						
VINDET detection voltage	$V_{VINGDDET}$	V_{VINDET} falling	945	960	975	mV
Hysteresis on $V_{VINGDDET}$	$V_{VINGDDET\_HYS}$		-	40	-	mV
VINDET input current	I_{VINDET}		-40	-	40	nA
SYSGD detection voltage	$V_{SYSGDDET}$	V_{SYSDET} rising	740	760	780	mV
Hysteresis on $V_{SYSGDDET}$	$V_{SYSGDDET\_HYS}$		-	20	-	mV
SYSGD detection deglitch time	t_{SYSDET}		-	100	-	µs
SYSDET input leakage current	I_{SYSDET}		-40	-	40	nA
SCAPGD detection voltage	$V_{SCAPDET}$	V_{CHGFB} rising, As Percentage to $V_{FB(CHG)}$	91.25	92.5	93.75	%
Hysteresis on $V_{SCAPDET}$	$V_{SCAPDET\_HYS}$		-	2.5	-	%
SCAPGD detection deglitch time	$t_{SCAPDET}$		-	100	-	µs
CHARGE PUMP FOR EXTERNAL FET						
INSW output voltage	$V_{INSWOUT}$		V_{VIN} × 1.77	V_{VIN} × 1.88	V_{VIN} × 1.99	V
INSW current capability	I_{INSW}	V_{INSW} = $V_{INSWOUT}$ × 0.9	-	5	-	µA
INPUT OVER VOLTAGE PROTECTION						
Input OVP voltage	V_{INOVP}	V_{VIN} rising	6.0	6.3	6.6	V
Release voltage on V_{INOVP}	V_{INOVP_REL}	V_{VIN} falling	5.6	5.7	5.8	V
INPUT OVER CURRENT PROTECTION						
Input OCP detection voltage	V_{INOCP}	(V_{CSP} - V_{CSN}) rising	30	40	50	mV
Input OCP detection deglitch time	t_{INOCP}		-	5	-	ms
THERMAL SHUTDOWN						
Thermal shutdown temperature	T_{SHUT}	Temperature increasing	-	160	-	°C
Hysteresis on T_{SHUT}	T_{SHUT_HYS}		-	15	-	°C
LOGIC INPUT AND OUTPUT						
Low level input voltage	V_{ILO}	CELL pin, CHGENB pin, BAKENB pin, FAULTB pin	-	-	0.4	V
High level input voltage	V_{IHI}	CELL pin, CHGENB pin, BAKENB pin, FAULTB pin	1.3	-	-	V

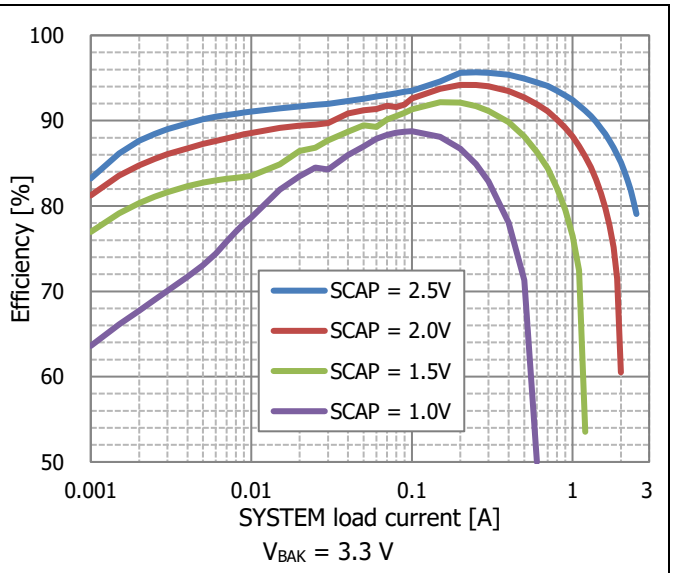
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output voltage at sink	V_{OL}	VINGD pin, SYSGD pin, SCAPGD pin, ALARMB pin at low, Sink current = 5 mA	-	-	0.4	V
Input leakage current	I_{LEAK}	VINGD pin, SYSGD pin, SCAPGD pin, ALARMB pin, FAULTB pin at Hi-Z, Pin = 5 V	-	-	1	µA
FAULTB pulldown current	$I_{PULLDOWN}$	V_{FAULTB} = 0.4 V	6	10	14	µA

7. TYPICAL CHARACTERISTICS



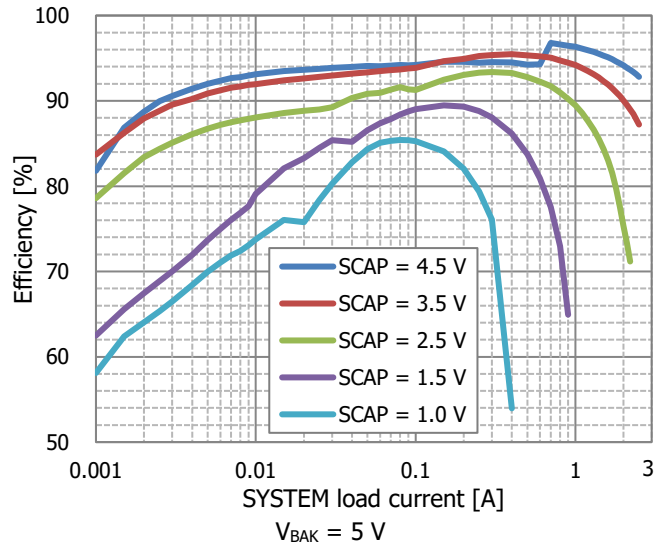
V_{VIN} = 5 V

Figure 1. Charging Efficiency vs. V_{SCAP}



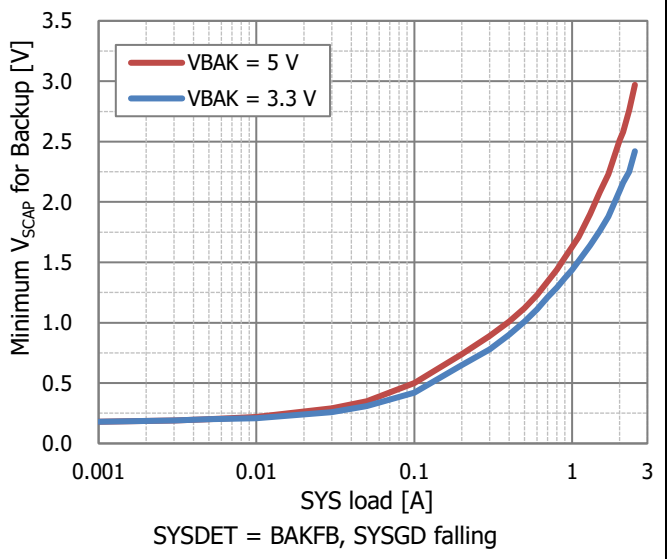
V_{BAK} = 3.3 V

Figure 2. Backup Efficiency vs. SYSTEM load 1



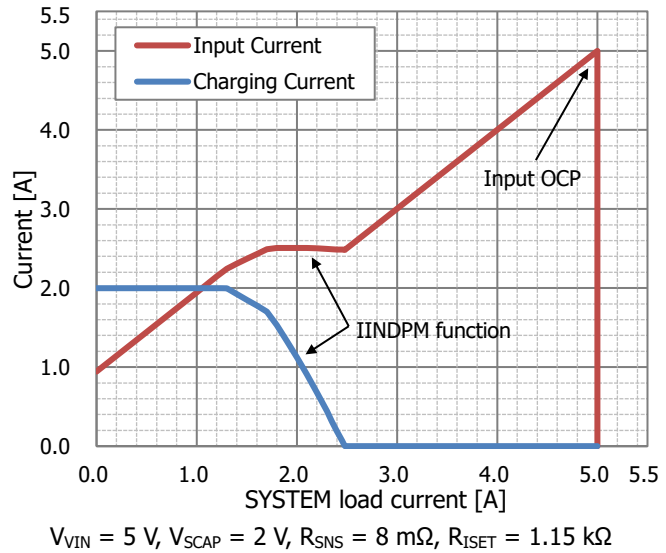
V_{BAK} = 5 V

Figure 3. Backup Efficiency vs. SYSTEM load 2



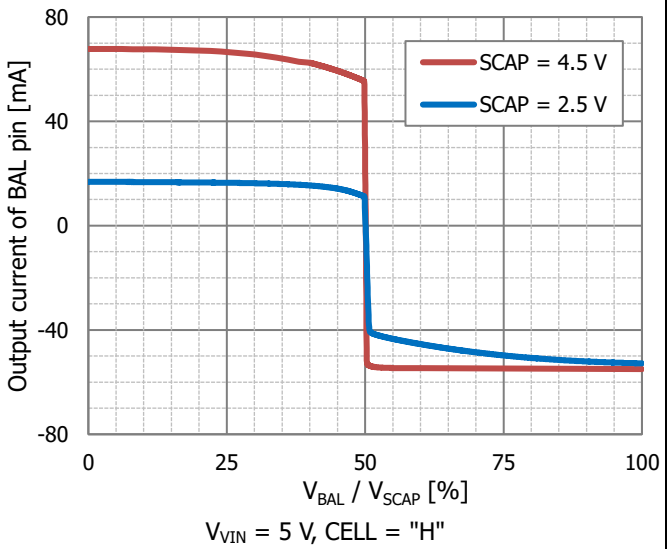
SYSDET = BAKFB, SYSGD falling

Figure 4. Minimum V_{SCAP} for Backup vs. SYSTEM load



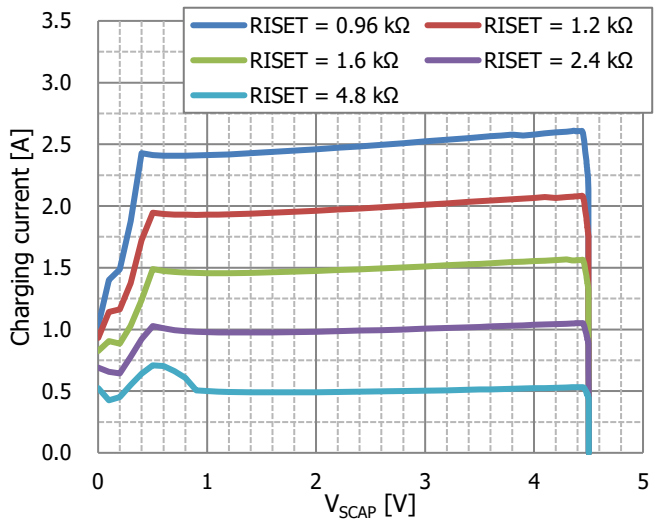
V_{VIN} = 5 V, V_{SCAP} = 2 V, R_{SNS} = 8 mΩ, R_{ISET} = 1.15 kΩ

Figure 5. IINDPM function and Input OCP



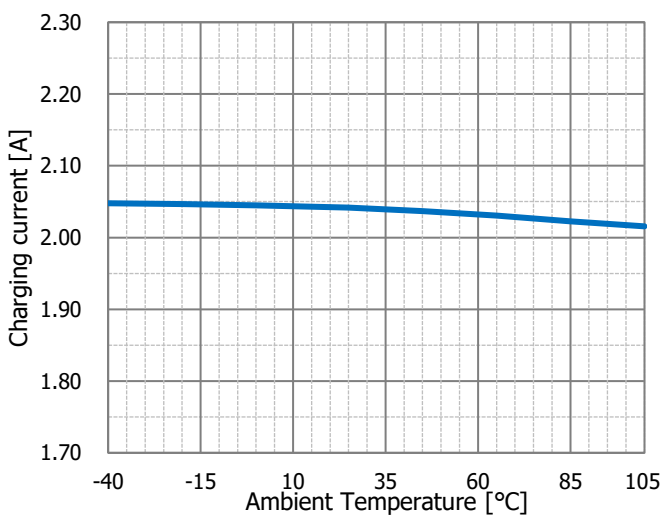
V_{VIN} = 5 V, CELL = "H"

Figure 6. Output current of BAL pin at Cell balance



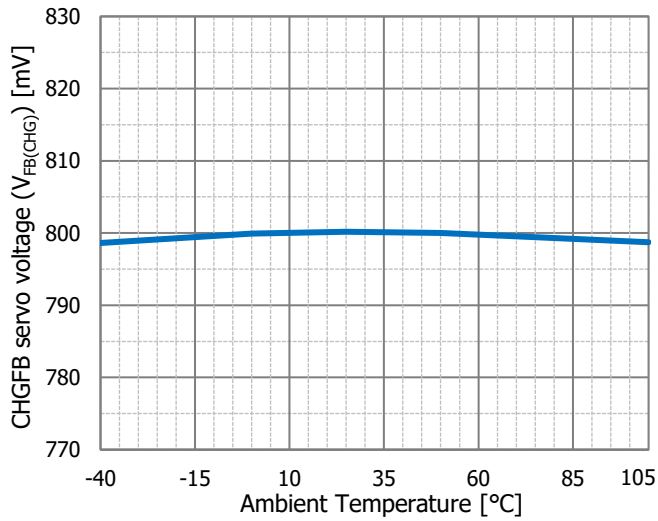
V_{VIN} = 5 V, V_{REG} = 4.5 V

Figure 7. Charging current vs. V_{SCAP}



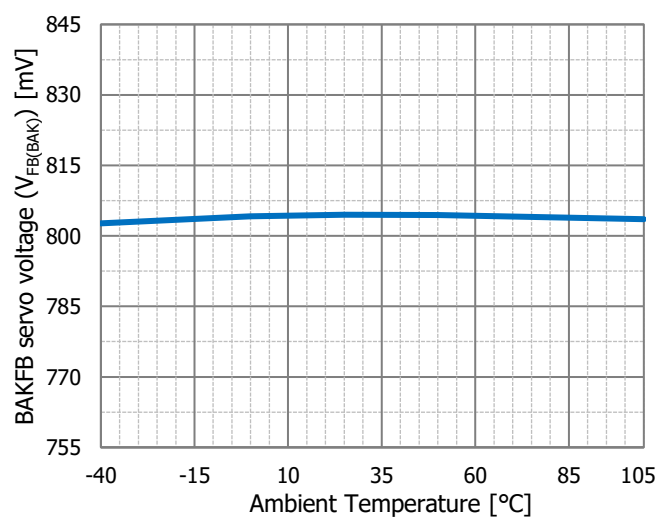
V_{VIN} = 5 V, V_{SCAP} = 2.8 V, R_{ISET} = 1 kΩ

Figure 8. Charging current vs. Ambient temp.



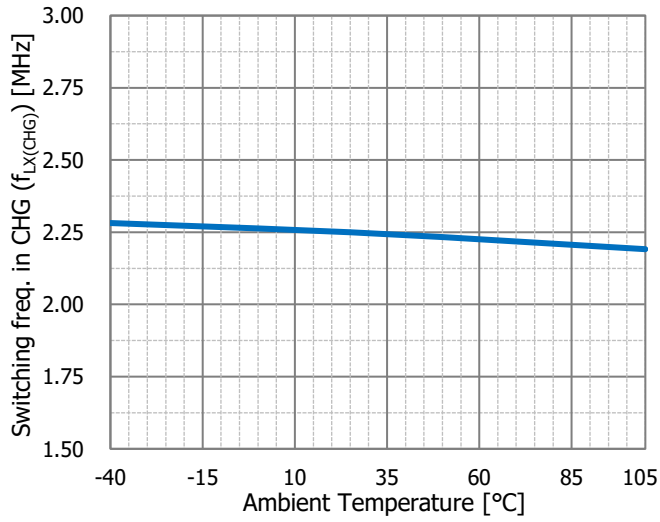
V_{VIN} = 5 V

Figure 9. CHGFB servo voltage vs. Ambient temp.



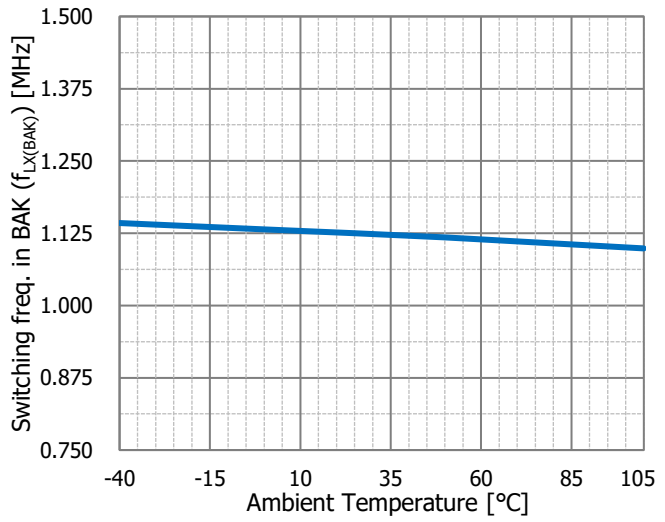
V_{BAK} = 5 V

Figure 10. BAKFB servo voltage vs. Ambient temp.



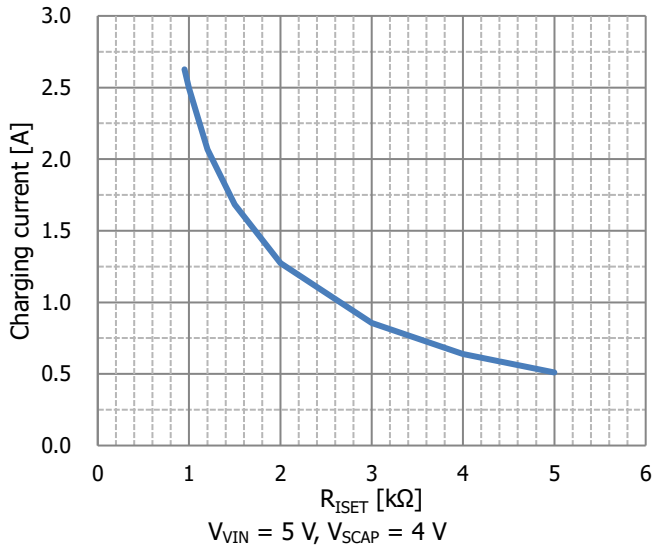
V_{VIN} = 5 V

Figure 11. Switching freq. in Charge vs. Ambient temp.



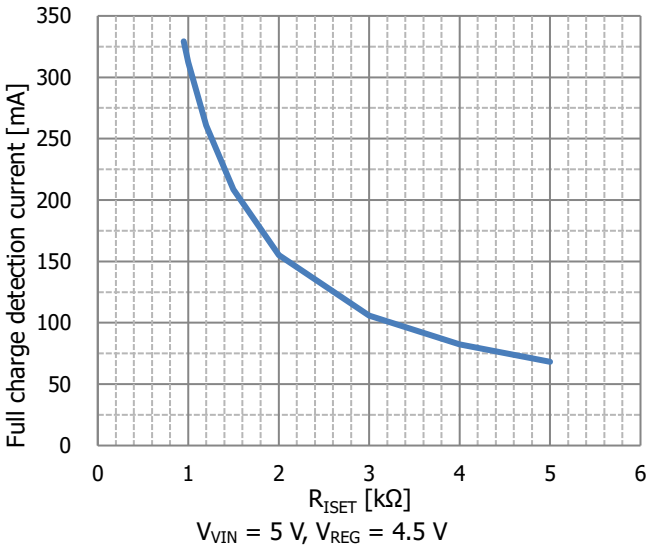
V_{BAK} = 5 V

Figure 12. Switching freq. in Backup vs. Ambient temp.



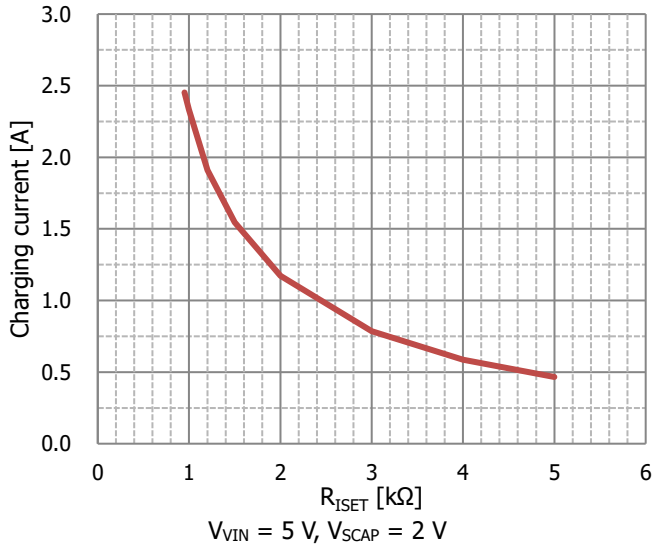
V_{VIN} = 5 V, V_{SCAP} = 4 V

Figure 13. Charging current vs. R_{ISET} 1



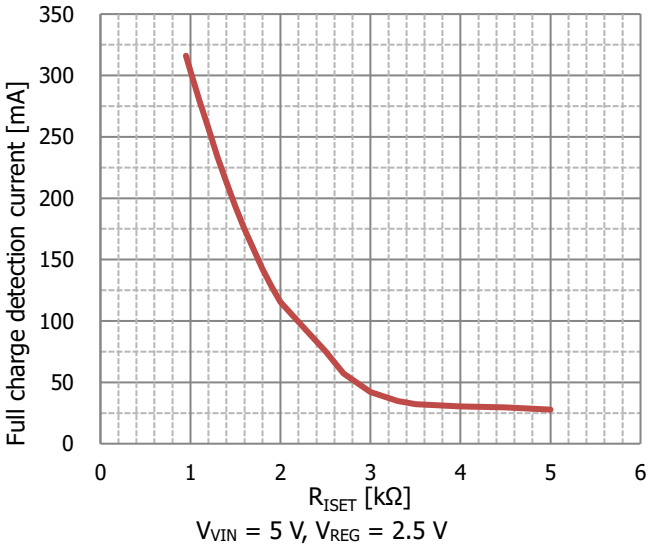
V_{VIN} = 5 V, V_{REG} = 4.5 V

Figure 14. Full charge detection current vs. R_{ISET} 1



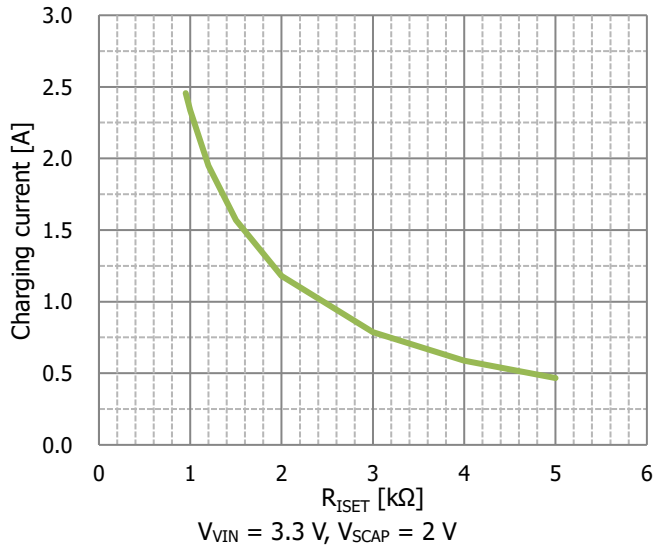
V_{VIN} = 5 V, V_{SCAP} = 2 V

Figure 15. Charging current vs. R_{ISET} 2



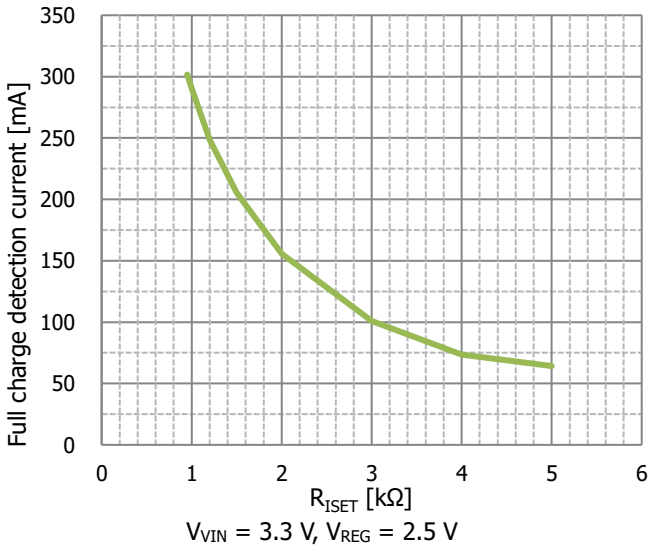
V_{VIN} = 5 V, V_{REG} = 2.5 V

Figure 16. Full charge detection current vs. R_{ISET} 2



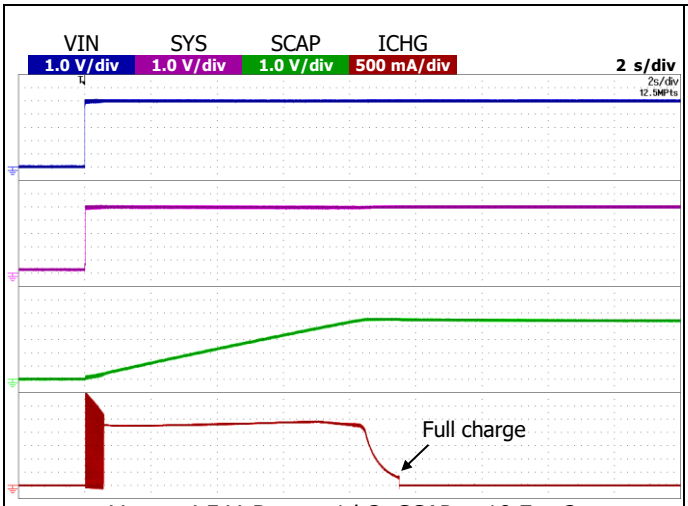
V_{VIN} = 3.3 V, V_{SCAP} = 2 V

Figure 17. Charging current vs. R_{ISET} 3



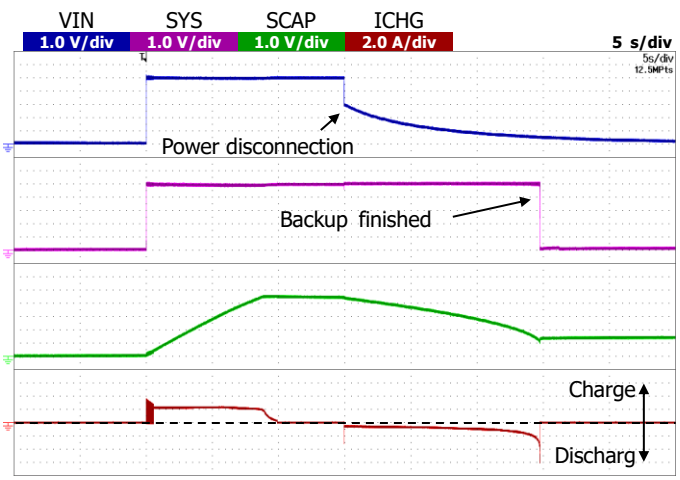
V_{VIN} = 3.3 V, V_{REG} = 2.5 V

Figure 18. Full charge detection current vs. R_{ISET} 3



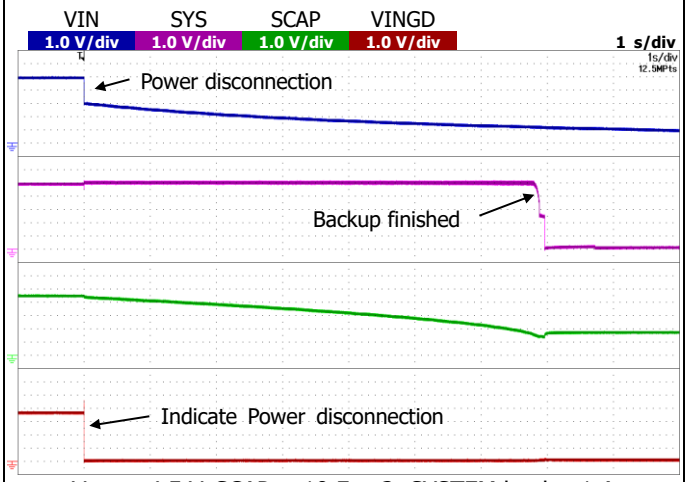
V_{REG} = 4.5 V, R_{ISET} = 1 kΩ, SCAP = 10 F × 2
V_{VIN} = OPEN to 5 V

Figure 19. Power on and Charging mode



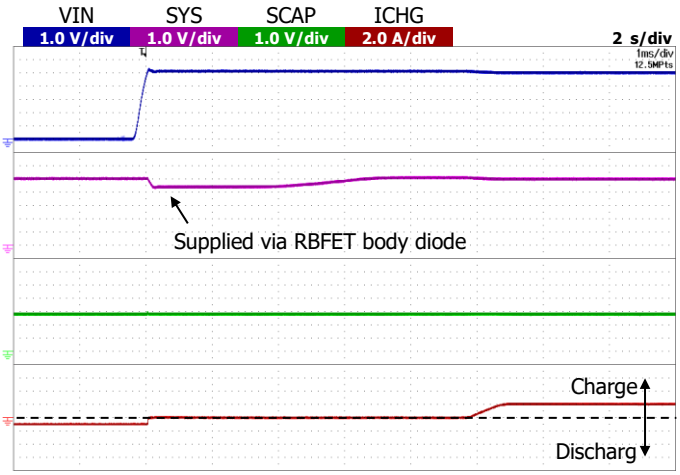
V_{REG} = 4.5 V, R_{ISET} = 1 kΩ, SCAP = 10 F × 2,
SYSTEM load = 500 mA, V_{VIN} = OPEN to 5 V to OPEN

Figure 20. Power on and disconnection



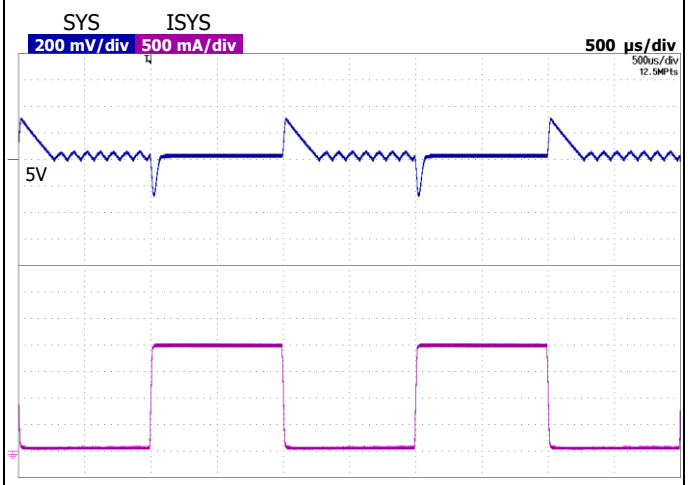
V_{REG} = 4.5 V, SCAP = 10 F × 2, SYSTEM load = 1 A
V_{VIN} = 5 V to OPEN

Figure 21. Power disconnection and Backup mode



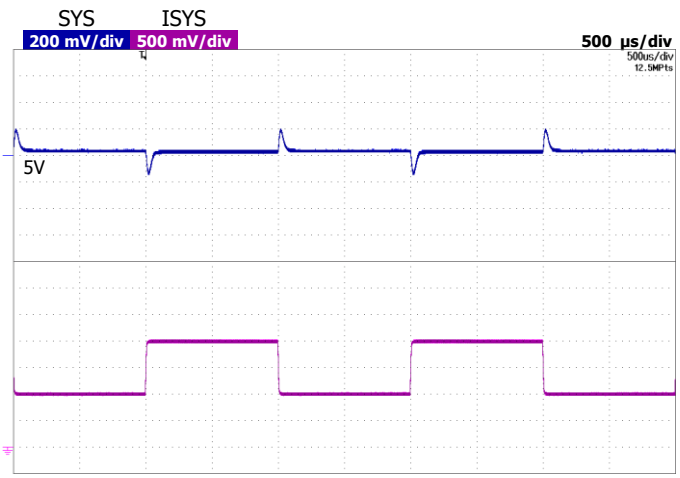
V_{SCAP} = 2.8 V, V_{BAK} = 5.0 V, without PFFET
V_{VIN} = OPEN to 5 V

Figure 22. Power connection during backup w/o PFFET



V_{SCAP} = 3.5 V, V_{BAK} = 5.0 V, C_{SYS} = 100 µF, L = 2.2 µH
SYSTEM load = 50 mA to 2 A to 50 mA

Figure 23. Transient response in Backup mode 1



V_{SCAP} = 3.5 V, V_{BAK} = 5.0 V, C_{SYS} = 100 µF, L = 2.2 µH
SYSTEM load = 1 A to 2 A to 1 A

Figure 24. Transient response in Backup mode 2

8. DESCRIPTION OF FUNCTIONS

The MM4039 is a supercapacitor charging/discharging control IC for power supply backup in 3.3 V and 5 V systems.
It charges the supercapacitor while providing power from the input power supply to the system, and if the input power supply is lost, it seamlessly shifts over to backup operation, wherein power is supplied from the supercapacitor to the system. Embedded with a charge pump circuit for driving the external NchFET of the input load switch, a charging buck DC-DC converter, and a backup boost DC-DC converter, it enables you to easily created power supply backup circuits. The DC-DC converters are both synchronous rectifier types with backflow prevention, and are highly efficient. The product supports one-cell and two-cell supercapacitors, and is embedded with a cell balance function for two-cell usage.

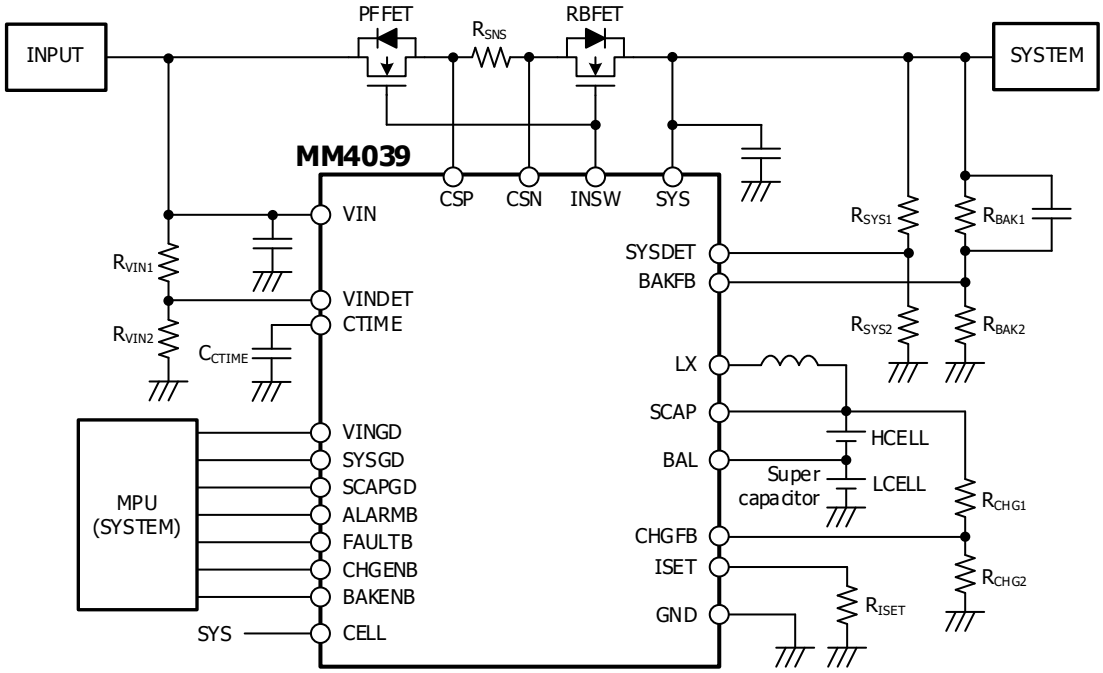


Figure 25. Typical circuit example

8-1. CELL pin

The MM4039 supports one-cell and two-cell supercapacitor, and this is selected based on the CELL pin.

- For one-cell supercapacitor: Connect the CELL pin to GND, and use CELL = "L".
- For two-cell supercapacitor: Connect the CELL pin to SYS, and use CELL = "H".

8-2. Input Power Supply Detection

The MM4039 judges whether an input power supply is connected or not based on the voltage at the VINDET pin. It operates in charging mode if a power supply is connected, and in backup mode if not. The input power supply detection threshold value (=$V_{INDETTH}$) is set by the external resistance R_{VIN1} and R_{VIN2}.

$$V_{INDETTH} = V_{VINGDDET} \times (1 + (R_{VIN1} / R_{VIN2}))$$

8-3. Charging Mode

If the input voltage exceeds the input power supply detection threshold value (=$V_{INDETTH}$), the charge pump is activated and the external NchFET is turned ON, beginning power supply from the input power supply to the system load.

While the external NchFET is ON, if the two conditions below are simultaneously met, then the charging buck DC-DC converter charges the supercapacitor, using the SYS pin as the power supply.

- The charging operation is enabled at the CHGENB pin. (CHGENB = "L")
- The SYS voltage is higher than the SCAP voltage. ($V_{SYS} > V_{SCAP} + V_{UVLO(CHG)}$)

8-3-1. CCCV Charging

The CCCV charging operation is performed using the charging current (=I_{CHG}) set by the external resistance R_{ISET} and the charging control voltage (=V_{REG}) set by the external resistance R_{CHG1} and R_{CHG2}.

$$I_{CHG} = 2400 / R_{ISET}$$
$$V_{REG} = V_{FB(CHG)} \times (1 + (R_{CHG1} / R_{CHG2}))$$

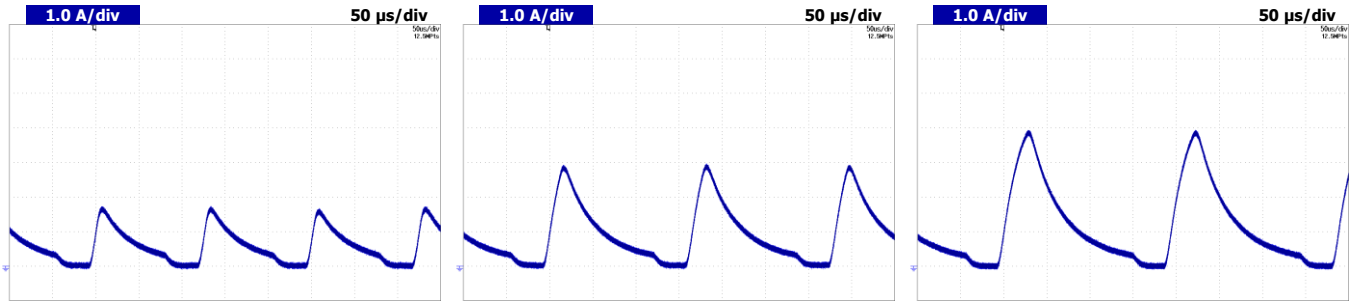
IINDPM Function

The charging current is reduced and the power supply to the system load is prioritized so that the sum of the system load current and the SYS current for charging does not exceed the input current limit (=I_{INLIM}) set by the external resistance R_{SNS}.

$I_{INLIM} = V_{IINDPM} / R_{SNS}$

Charging Current at Low SCAP Voltage

If the SCAP voltage is low (V_{SCAP} < 1 V), the charging buck DC-DC converter becomes unable to maintain the linearity of the PWM control. Therefore, the output current may overshoot or undershoot the set I_{CHG}.



V_{VIN} = 5 V, V_{SCAP} = 0 V, I_{CHG} = 500 mA V_{VIN} = 5 V, V_{SCAP} = 0 V, I_{CHG} = 1500 mA V_{VIN} = 5 V, V_{SCAP} = 0 V, I_{CHG} = 2500 mA

Figure 26. Charge current waveform at low SCAP voltage

8-3-2. Full Charge

In CV charging operation, the charging current decreases. In conjunction with this, the ISET voltage decreases. When the ISET voltage becomes equal or less than the full charge detection voltage (=V_{EOC}) (deglitch time: t_{EOC}), the charge is deemed full and the charging operation stops. See Figure 14, Figure 16 and Figure 18 on page 11 for the charge current values at which a full charge is determined. If the charging current is decreased by the IINDPM function, the judgment for full charges is not performed.

8-3-3. Recharging

After a full charge, if the CHGFB voltage is detected (deglitching time: t_{RECHG}) to have fallen below the recharging detection voltage (=V_{RECHG}), the charging operation is restarted.

8-3-4. Cell Balance Function

During the charging mode when CELL = "H" (two-cell selection), servo control is performed on the BAL pin to the cell balance control voltage (=V_{BALV}) in order to equalize the voltages of HCELL and LCELL of the supercapacitor. The source function and the sink function of the BAL pin correspond to $I_{BALSOURCE}$ and $I_{BALSINK}$, respectively. The cell balance function operates during CCCV charging and during a full charge.
When CELL = "L" (one-cell selection), this function does not operate. Leave the BAL pin open, or connect it to GND.

8-4. Backup Mode

If the input voltage falls below the input power supply detection threshold value (=$V_{INDETTH}$), the charge pump is stopped and the external NchFET is turned OFF.

While the external NchFET is OFF, if the two conditions below are simultaneously met, then the backup boost DC-DC converter starts up and supplies power to the system load (performs the backup operation), using the supercapacitor as the power supply.

- The backup operation is enabled at the BAKENB pin. (BAKENB = "L")
- The SYS voltage or SCAP voltage is higher the UVLO during backup. ((V_{SYS} or V_{SCAP}) > $V_{UVLO(BAK)}$)

The backup output voltage (=V_{BAK}) is set by the external resistance R_{BAK1} and R_{BAK2}.

$V_{BAK} = V_{FB(BAK)} \times (1 + (R_{BAK1} / R_{BAK2}))$

In backup mode, the product automatically shifts to PFM control if a light load is detected in order to improve efficiency under light loads.

Mode Switching Dead Time

When transitioning from charging mode to backup mode, ringing may occur on the input side due to the sudden stop of current from the input power supply to the system load. To prevent this ringing from causing repeated switching between charging and backup modes, a dead time is provided immediately after switching to backup mode. During this time, the device is in backup mode and the VIN pulldown resistance (=$R_{VINPULL}$) on the VIN pin is activated, discharging the VIN. The dead time for

switching to this mode (=t_{CTIME}) is determined by the external capacitance C_{CTIME}.

$t_{CTIME} = C_{CTIME} \times 1.9 \times 10^6$

8-5. Shutdown Mode

Setting both the CHGENB and BAKENB pins to "H" will put the product into shutdown mode. In this mode, the charge pump, external NchFET, charging buck DC-DC converter, and backup boost DC-DC converter will stop operating, regardless of the input voltage or supercapacitor voltage.

8-6. Voltage Detection Indicators

8-6-1. VINGD pin

The VINGD pin is the VINDET voltage indicator for the NMOS open drain output. If the VINDET voltage exceeds the VINDET detection voltage (=$V_{VINGDDET}$), then "Hi-Z" is output, and if it falls below it, then "Low" is output.

8-6-2. SYSGD pin

The SYSGD pin is the SYSDET voltage indicator for the NMOS open drain output. If the SYSDET voltage is detected (deglitching time: t_{SYSDET}) as having exceeded the SYSGD detection voltage (=$V_{SYSGDDET}$), then "Hi-Z" is output, and if it is detected (deglitching time: t_{SYSDET}) as having fallen below it, then "Low" is output.

8-6-3. SCAPGD pin

The SCAPGD pin is the CHGFB voltage indicator for the NMOS open drain output. If the CHGFB voltage is detected (deglitching time: $t_{SCAPDET}$) as having exceeded the SCAPGD detection voltage (=$V_{SCAPDET}$), then "Hi-Z" is output, and if it is detected (deglitching time: $t_{SCAPDET}$) as having fallen below it, then "Low" is output.

8-7. Protect Functions

The MM4039 is embedded with supercapacitor protection, system protection, and DC-DC converter protection. It can prevent device damage even if errors such as shorted pins occur.

8-7-1. Supercapacitor Protection (FAULTB pin)

The supercapacitor protection includes the "Charging Mode SCAP Overvoltage Protection" and the "Backup Mode SCAP Overdischarge Protection", and the FAULTB pin is the indicator. The FAULTB pin is the NMOS open drain output. Under normal conditions, it outputs "Hi-Z", and when the protective function operates, it performs a pulldown using the FAULTB pin pulldown current (=$I_{PULLDOWN}$) and outputs "Low".
If you will not use the supercapacitor protective functions, apply the "H" voltage to the FAULTB pin.

Charging Mode SCAP Overvoltage Protection

During charging mode, if the supercapacitor voltage exceeds the charging overvoltage detection voltage (=$V_{SCAPOVP}$), the charging buck DC-DC converter stops and the FAULTB pin is set to "Low". Overvoltage monitoring is performed separately for HCELL and for LCELL. This is an automatic-recovery type.

Backup Mode SCAP Overdischarge Protection

During backup mode when CELL = "H" (two-cell selection), if the supercapacitor voltage falls below the backup input low voltage detection voltage (=$V_{SCAPLVP}$), the backup boost DC-DC converter stops and the FAULTB pin is set to "Low". Overdischarge monitoring is performed separately for HCELL and for LCELL. This is an automatic-recovery type.
When CELL = "L" (one-cell selection), this function does not operate.

8-7-2. System Protection (ALARMB pin)

The system protection includes the "Input Overvoltage Protection", the "Input Overcurrent Protection", and the "Thermal Shutdown", and the ALARMB pin is the indicator. The ALARMB pin is the NMOS open drain output. Under normal circumstances, it outputs "Hi-Z", and when the protective function operates, it outputs "Low".

Input Overvoltage Protection

If the VIN voltage exceeds the input OVP voltage (=V_{INOVP}), the charge pump is stopped and the external NchFET is turned OFF. Furthermore, the charging buck DC-DC converter and backup boost DC-DC converter also stop. This is an automatic-recovery type.

Input Overcurrent Protection

If an input current exceeding the input overcurrent value (=I_{INOCP}) set by the external resistance R_{SNS} is detected (deglitching time: t_{INOCP}), then the charge pump output is stopped and the external NchFET is turned OFF. Furthermore, the charging buck DC-DC converter and backup boost DC-DC converter also stop. This is a latch-off type. In order to release the latch, it must be deemed that there is no power supply connected by "Input Power Supply Detection" on page 13.

$I_{INOCP} = V_{INOCP} / R_{SNS}$

Thermal Shutdown

In order to prevent thermal destruction, a thermal shutdown circuit is embedded. If the junction temperature exceeds the thermal shutdown temperature (=T_{SHUT}), then the charge pump output is stopped and the external NchFET is turned OFF. Furthermore, the charging buck DC-DC converter and backup boost DC-DC converter also stop. This is an automatic-recovery type.
Furthermore, the thermal shutdown is a function that operates in a range exceeding the absolute maximum rating. Therefore, please avoid proactively using this function.

8-7-3. DC-DC Converter Protection

Charging Buck DC-DC Converter Output Overvoltage Protection

Refer to "Charging Mode SCAP Overvoltage Protection" on page 15.

Charging Buck DC-DC Converter Overcurrent Protection

In charging mode, if the current that flows through the embedded FET exceeds the charging overcurrent detection current (=$I_{OCP(CHG)}$), the switching operation is stopped. This is an automatic-recovery type.

Backup Boost DC-DC Converter Output Overvoltage Protection

In backup mode, if the SYS voltage exceeds the backup output overvoltage detection voltage (=V_{SYSOVP}), the switching operation is stopped. This is an automatic-recovery type.

Backup Boost DC-DC Converter Overcurrent Protection

In backup mode, if the current that flows through the embedded FET exceeds the backup overcurrent detection current (=$I_{OCP(BAK)}$), the switching operation is stopped. This is an automatic-recovery type.

9. APPLICATION CIRCUIT EXAMPLE

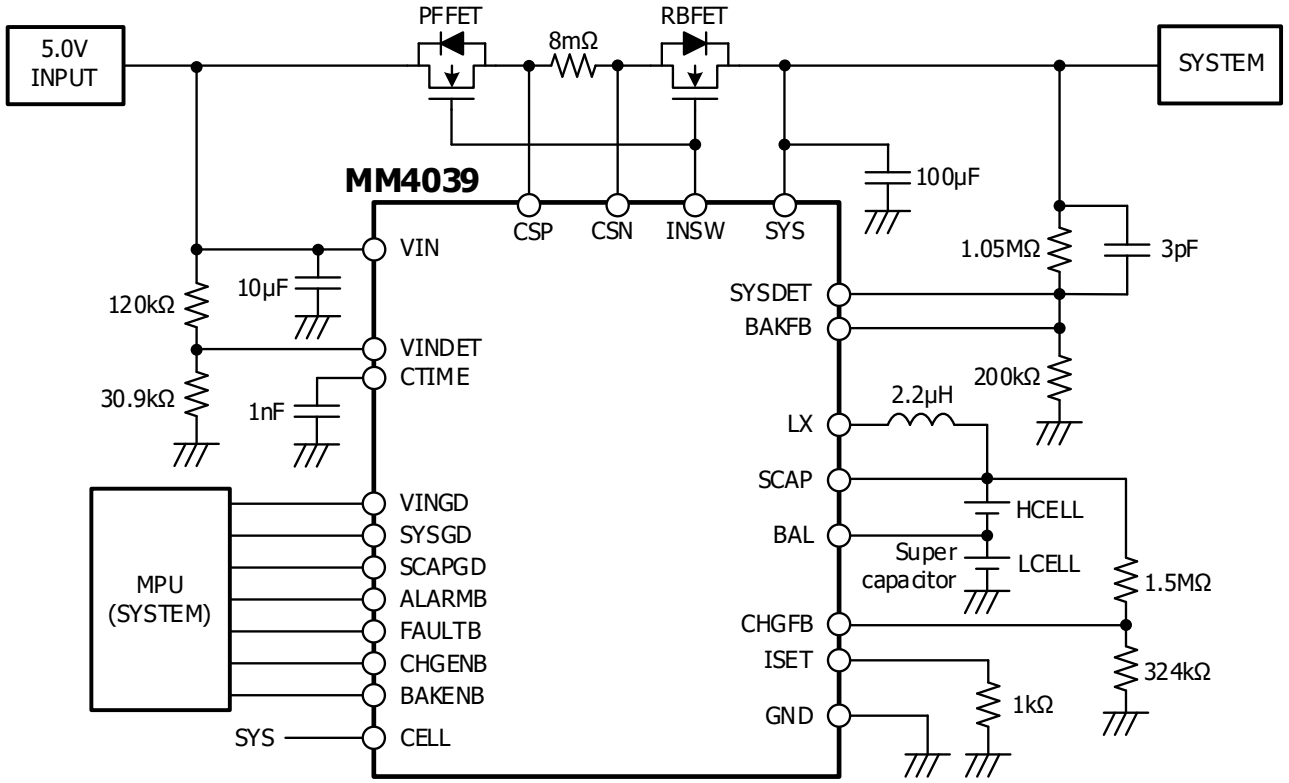


Figure 27. 5 V system, Supercapacitor two-cell

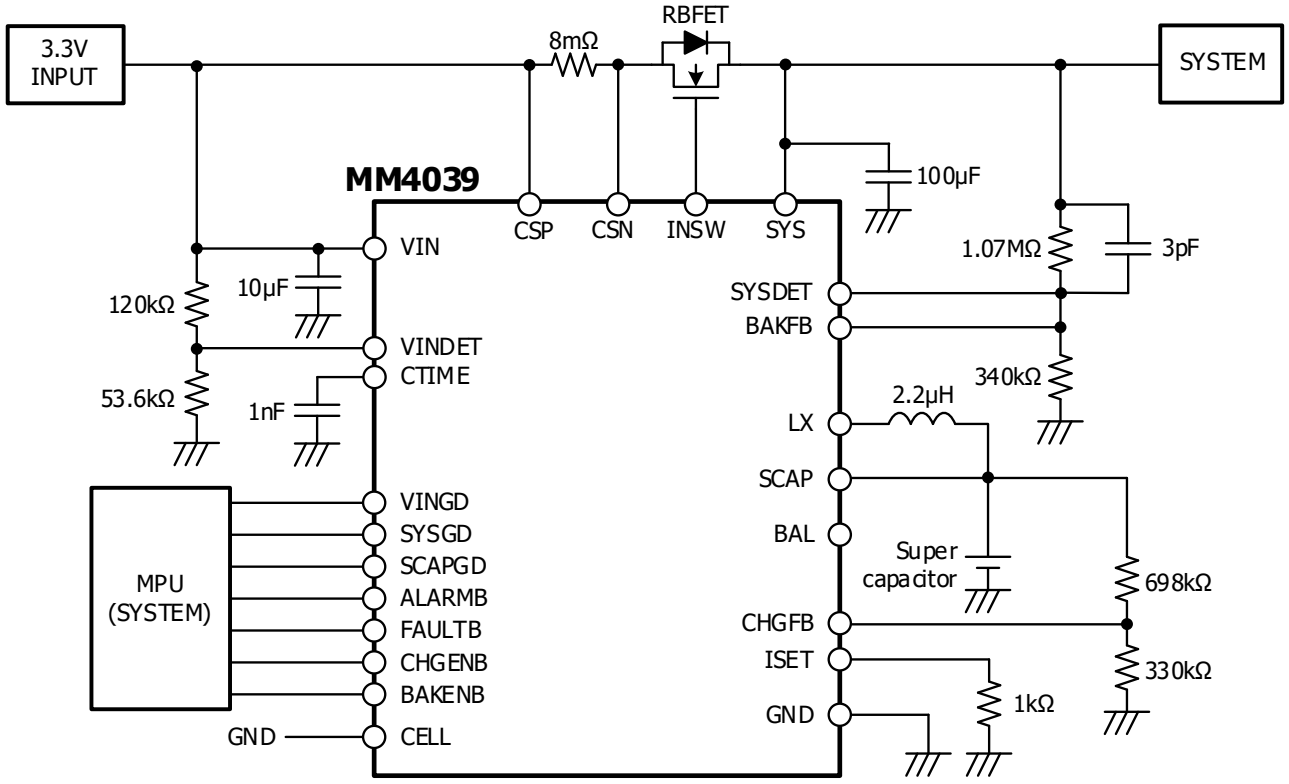
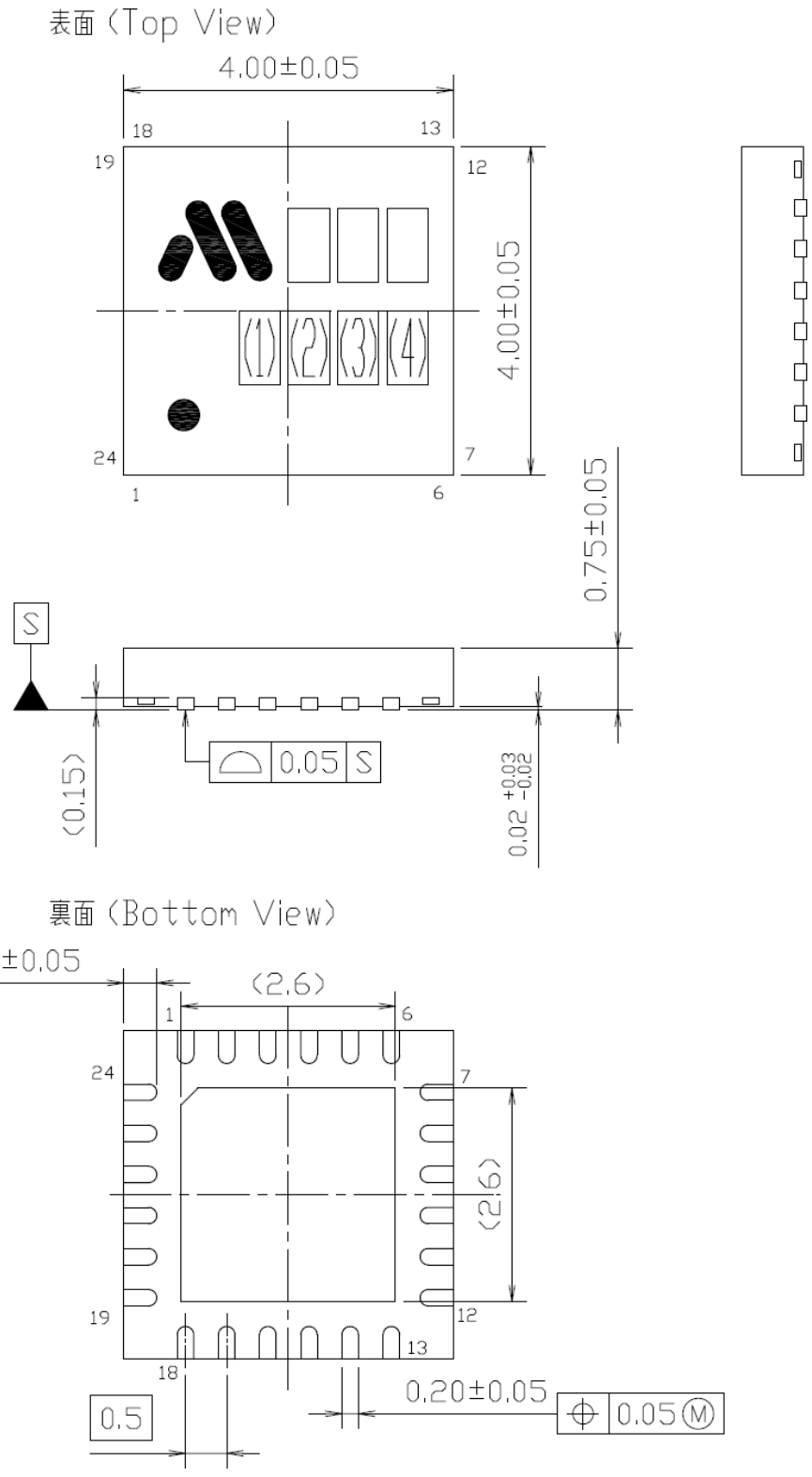


Figure 28. 3.3 V system, Supercapacitor one-cell without input-OVP function

10. DIMENSIONS

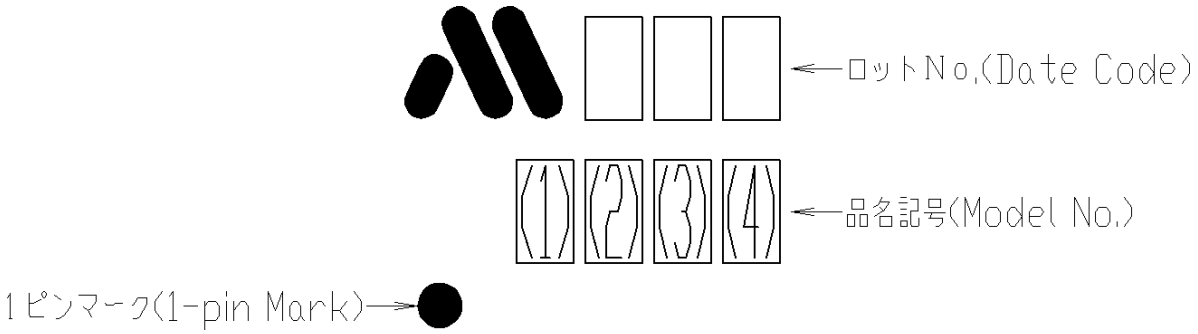
PACKAGE : SQFN-24A

UNIT	mm



No. SEM.-SP-R24A-0001

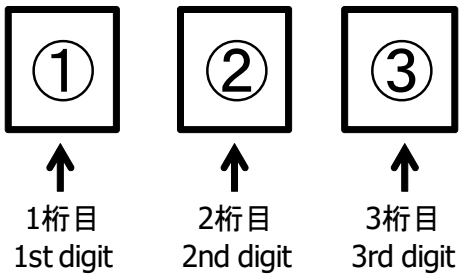
11. MARKING CONTENTS



Model name	Model No.			
	(1)	(2)	(3)	(4)
MM4039XRRE	0	3	9	X

3桁ロットNo. 判別方法

How to identify 3 characteristic lot numbers.



(1) ロットNo. の1桁目 (①)は生産年(西暦)の末尾を示す。
The 1st digit (①) shows the last digit of a production year (western calendar).

(2) 2桁目(②)、及び3桁目(③)の数字は、量産に於ける生産週を示す。
The 2nd (②) and 3rd (③) digit show a production week of mass production.

【生産年の表記方法/How to indicate a production year】

1桁目(①)/The 1st digit (①)	
西暦年末尾 the last digit of a production year	使用表示文字 mark
xxx1	1
xxx2	2
xxx3	3
xxx4	4
xxx5	5
xxx6	6
xxx7	7
xxx8	8
xxx9	9
xxx0	0

2桁目、及び3桁目(②③)/The 2nd and 3rd digit (②③)			
生産週 production week	使用表示文字 mark	生産週 production week	使用表示文字 mark
1	01	27	27
2	02	28	28
3	03	29	29
4	04	30	30
5	05	31	31
6	06	32	32
7	07	33	33
8	08	34	34
9	09	35	35
10	10	36	36
11	11	37	37
12	12	38	38
13	13	39	39
14	14	40	40
15	15	41	41
16	16	42	42
17	17	43	43
18	18	44	44
19	19	45	45
20	20	46	46
21	21	47	47
22	22	48	48
23	23	49	49
24	24	50	50
25	25	51	51
26	26	52	52
		53	53